APPARATUS, SYSTEM, AND METHOD FOR DOWN-CONVERTING AND UP-CONVERTING ELECTROMAGNETIC SIGNALS

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of pending U.S. Patent Application 09/550,644, filed April 14, 2000, which is herein incorporated by reference in its entirety, and this application claims the benefit of U.S. Provisional Application 60/204,796, filed May 16, 2000, U.S. Provisional Application 60/213,363, filed June 21, 2000, and U.S. Provisional Application 60/272,043, filed March 1, 2001, all of which and are herein incorporated by reference in their entireties.

[0002] The following patents and patent applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

[0003] U.S. Patent No. 6,061,551, entitled "Method and System for Down-Converting Electromagnetic Signals," filed October 21, 1998 and issued May 9, 2000.

[0004] U.S. Patent No. 6,091,940, entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998 and issued July 18, 2000.

[0005] U.S. Patent No. 6,061,555, entitled "Method and System for Ensuring Reception of a Communications Signal," filed October 21, 1998 and issued May 9, 2000.

[0006] U.S. Patent No. 6,049,706, entitled "Integrated Frequency Translation And Selectivity," filed October 21, 1998 and issued April 11, 2000.

[0007] "Applications of Universal Frequency Translation," Ser. No. 09/261,129, filed March 3, 1999.

[0008] "Method, System, and Apparatus for Balanced Frequency Up-Conversion of a Baseband Signal," Ser. No. 09/525,615, filed March 14, 2000.

BACKGROUND OF THE INVENTION

Field of the Invention

[0009] The present invention relates generally to the down-conversion and up-conversion of an electromagnetic signal using a universal frequency translation module.

Related Art

[0010] Various communication components exist for performing frequency down-conversion, frequency up-conversion, and filtering. Also, schemes exist for signal reception in the face of potential jamming signals.

SUMMARY OF THE INVENTION

[0011] Briefly stated, the present invention is directed to methods, systems, and apparatuses for down-converting and/or up-converting an electromagnetic signal, and applications thereof.

[0012] In an embodiment, the invention down-converts the electromagnetic signal to an intermediate frequency signal.

[0013] In another embodiment, the invention down-converts the electromagnetic signal to a demodulated baseband information signal.

[0014] In another embodiment, the electromagnetic signal is a frequency modulated (FM) signal, which is down-converted to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal.

[0015] In one embodiment, the invention uses a stable, low frequency signal to generate a higher frequency signal with a frequency and phase that can be used as stable references.

[0016] In another embodiment, the present invention is used as a transmitter. In this embodiment, the invention accepts an information signal at a baseband frequency and transmits a modulated signal at a frequency higher than the baseband frequency.

[0017] In an embodiment, the invention operates by receiving an electromagnetic signal and recursively operating on approximate half cycles of a carrier signal. The recursive operations are typically performed at a sub-harmonic rate of the carrier signal. The invention accumulates the results of the recursive operations and uses the accumulated results to form a down-converted signal.

[0018] The methods and systems of transmitting vary slightly depending on the modulation scheme being used. For some embodiments using frequency modulation (FM) or phase modulation (PM), the information signal is used to modulate an oscillating signal to create a modulated intermediate signal. If needed, this modulated intermediate signal is "shaped" to provide a substantially optimum pulse-width-to-period ratio. This shaped signal is then used to control a switch that opens and closes as a function of the frequency and pulse width of the shaped signal. As a result of this opening and closing, a signal that is harmonically rich is produced with each harmonic of the harmonically rich signal being modulated substantially the same as the modulated intermediate signal. Through proper filtering, the desired harmonic (or harmonics) is selected and transmitted.

[0019] For some embodiments using amplitude modulation (AM), the switch is controlled by an unmodulated oscillating signal (which may, if needed, be shaped). As the switch opens and closes, it gates a reference signal, which is the information signal. In an alternate implementation, the information signal is combined with a bias signal to create the reference signal, which is then gated. The result of the gating is a harmonically rich signal having a fundamental frequency substantially proportional to the oscillating signal and an amplitude substantially proportional to the amplitude of the reference signal. Each of the harmonics of the harmonically rich signal also has

amplitudes proportional to the reference signal, and is thus considered to be amplitude modulated. Just as with the FM/PM embodiments described above, through proper filtering, the desired harmonic (or harmonics) is selected and transmitted.

[0020] The invention is applicable to any type of electromagnetic signal, including but not limited to, modulated carrier signals (the invention is applicable to any modulation scheme or combination thereof) and unmodulated carrier signals.

[0021] Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented herein for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

BRIEF DESCRIPTION OF THE FIGURES

[0022] The invention shall be described with reference to the accompanying figures, wherein:

[0023] FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

[0024] FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

[0025] FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention.

[0026] FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

[0027] FIG. 2 is a block diagram of a universal frequency translation (UFT) module according to an alternative embodiment of the invention.

[0028] FIGs. 3A and 3G are example aliasing modules according to embodiments of the invention.

[0029] FIGs. 3B-3F are example waveforms used to describe the operation of the aliasing modules of FIGs. 3A and 3G.

[0030] FIG. 4 illustrates an energy transfer system with an optional energy transfer signal module according to an embodiment of the invention.

[0031] FIG. 5 illustrates an example aperture generator.

[0032] FIG. 6A illustrates an example aperture generator.

[0033] FIG. 6B illustrates an oscillator according to an embodiment of the present invention.

[0034] FIGs. 7A-B illustrate example aperture generators.

[0035] FIG. 8 illustrates an aliasing module with input and output impedance match according to an embodiment of the invention.

[0036] FIG. 9 illustrates an example energy transfer module with a switch module and a reactive storage module according to an embodiment of the invention.

[0037] FIG. 10 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

[0038] FIG. 11 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

[0039] FIG. 12 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention.

[0040] FIGs. 13A-13I illustrate example waveforms used to describe the operation of the UFU module.

[0041] FIG. 14 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention.

[0042] FIG. 15 illustrates an exemplary I/Q modulation embodiment of a receiver according to the invention.

[0043] FIG. 16A is an example two-switch receiver according to an embodiment of the invention.

[0044] FIGs. 16B-16G are example waveforms used to describe the operation of the example two-switch receiver of FIG. 16A.

[0045] FIG. 16H is an example two-switch receiver according to an embodiment of the invention.

[0046] FIGs. 16I-16N are example waveforms used to describe the operation of the example two-switch receiver of FIG. 16H.

[0047] FIG. 16O is a two-switch receiver and optional amplifier according to an embodiment of the invention.

[0048] FIG. 17 is an example two-switch receiver according to an embodiment of the invention.

[0049] FIG. 18A is an example one-switch receiver according to an embodiment of the invention.

[0050] FIGs. 18B-18E are example waveforms used to describe the operation of the example one-switch receiver of FIG. 18A.

[0051] FIG. 19 is an example one-switch receiver according to an embodiment of the invention.

[0052] FIG. 20A is an example one-switch receiver according to an embodiment of the invention.

[0053] FIGs. 20B-20D are example waveforms used to describe the operation of the example one-switch receiver of FIG. 20A.

[0054] FIG. 20E is an example one-switch receiver according to an embodiment of the invention.

[0055] FIG. 20F is an example one-switch receiver according to an embodiment of the invention.

[0056] FIG. 21 is an example one-switch receiver according to an embodiment of the invention.

[0057] FIGs. 22-23 illustrate exemplary block diagrams of a transmitter operating in an I/Q modulation mode, according to embodiments of the invention.

[0058] FIG. 24A is an example two-switch transmitter according to an embodiment of the invention.

[0059] FIGs. 24B-24K are example waveforms used to describe the operation of the example two-switch transmitter of FIG. 24A.

[0060] FIG. 25A is an example two-switch transmitter according to an embodiment of the invention.

[0061] FIGs. 25B-25F are example waveforms used to describe the operation of the example two-switch transmitter of FIG. 25A.

[0062] FIG. 26A is an example two-switch transmitter according to an embodiment of the invention.

[0063] FIGs. 26B-26F are example waveforms used to describe the operation of the example two-switch transmitter of FIG. 26A.

[0064] FIG. 27A is an example one-switch transmitter according to an embodiment of the invention.

[0065] FIGs. 27B-27E are example waveforms used to describe the operation of the example one-switch transmitter of FIG. 27A.

[0066] FIG. 28 illustrates a block diagram of a transceiver implementation according to an embodiment of the present invention.

[0067] FIG. 29 illustrates an exemplary receiver using UFD conversion techniques according to an embodiment of the present invention.

[0068] FIG. 30 illustrates an exemplary transmitter according to an embodiment of the present invention.

[0069] FIGs. 31A, 31B, and 31C illustrate an exemplary transmitter according to an embodiment of the present invention in a transceiver circuit with a universal frequency down conversion receiver operating in a half-duplex mode for an FM and PM modulation embodiment.

[0070] FIG. 32 illustrates an exemplary half-duplex mode transceiver implementation according to an embodiment of the present invention.

[0071] FIG. 33 illustrates an exemplary full-duplex mode transceiver implementation according to an embodiment of the present invention.

[0072] FIG. 34 is an example one-switch transceiver according to an embodiment of the invention.

[0073] FIG. 35 is an example digital aperture generator circuit according to an embodiment of the invention.

[0074] FIG. 36 is an example modulated carrier signal.

[0075] FIG. 37 is an example control signal for a conventional receiver.

[0076] FIG. 38 is an example control signal according to the invention.

[0077] FIG. 39 illustrates an aperture and a voltage signal for a conventional receiver.

[0078] FIG. 40 illustrates an aperture and a voltage signal according to an embodiment of the invention.

[0079] FIG. 41 illustrates voltage signals according to embodiments of the invention.

[0080] FIG. 42 is a plot of FET drain current as a function of drain-source voltage in embodiments of the invention.

[0081] FIG. 43 illustrates how FET linearity is enhanced by increasing drain-source voltage in embodiments of the invention.

[0082] FIG. 44 illustrates how FET linearity is enhanced when gate-source voltage is made proportional to drain-source voltage in embodiments of the invention.

[0083] FIGs. 45A-E illustrates how FET drain current distortion is reduced in embodiments of the invention.

[0084] FIGs. 46-53 further illustrate how FET linearity is enhanced in embodiments of the invention.

[0085] FIGS. 54-56 illustrate example processor embodiments according to the present invention.

[0086] FIG. 57 illustrates the relationship between beta and the output charge of a processor according to an embodiment of the present invention.

[0087] FIG. 58 illustrates an RC processor according to an embodiment of the present invention coupled to a load resistance.

[0088] FIG. 59 illustrates an example implementation of the present invention.

[0089] FIG. 60 illustrates an example charge/discharge timing diagram according to an embodiment of the present invention.

[0090] FIG. 61 illustrates example energy transfer pulses (control signal) according to an embodiment of the present invention.

[0091] FIG. 62 illustrates a flowchart of a method for down-converting an electromagnetic signal according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Table of Contents

1. Introduction

[0092] The present invention is directed to the down-conversion and up-conversion of an electromagnetic signal using a universal frequency translation (UFT) module, transforms for same, and applications thereof. The systems described herein each may include one or more receivers, transmitters, and/or transceivers. According to embodiments of the invention, at least some of these receivers, transmitters, and/or transceivers are implemented using universal frequency translation (UFT) modules. The UFT modules perform frequency translation operations. Embodiments of the present invention are described below.

[0093] Systems that transmit and receive EM signals using UFT modules exhibit multiple advantages. These advantages include, but are not limited to, lower power consumption, longer power source life, fewer parts, lower cost, less tuning, and more effective signal transmission and reception. These systems can receive and transmit signals across a broad frequency range. The structure and operation of embodiments of the UFT module, and various applications of the same are described in detail in the following sections, and in the referenced documents.

2. Universal Frequency Translation

[0094] The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

[0095] FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

[0096] As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

[0097] Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

[0098] An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

[0099] As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label. Other embodiments, as described herein, have more than three ports.

[0100] The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

[0101] For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

[0102] As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this

capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

[0103] These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2.1 Frequency Down-Conversion

[0104] The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

[0105] In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," the full disclosure of which is incorporated herein by reference. A relevant portion of the above-mentioned patent is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal. The frequency translation aspects of the invention are further described in other documents referenced above, such as Application Ser. No. 09/550,644, entitled "Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships."

[0106] FIG. 3A illustrates an aliasing module 300 for down-conversion using a universal frequency translation (UFT) module 302 which down-converts an EM input signal 304. In particular embodiments, aliasing module 300 includes a switch 308 and a capacitor 310 (or integrator). (In embodiments, the UFT module is considered to include the switch and integrator.) The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 308 is in series with input signal 304 and capacitor

310 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 3G), the capacitor 310 is in series with the input signal 304 and the switch 308 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 300 with UFT module 302 can be tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 304.

[0107] In one implementation, aliasing module 300 down-converts the input signal 304 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 300 down-converts the input signal 304 to a demodulated baseband signal. In yet another implementation, the input signal 304 is a frequency modulated (FM) signal, and the aliasing module 300 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

[0108] In an embodiment, the control signal 306 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 304. In this embodiment, the control signal 306 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 304. Preferably, the frequency of control signal 306 is much less than the input signal 304.

[0109] A train of pulses 318 as shown in FIG. 3D controls the switch 308 to alias the input signal 304 with the control signal 306 to generate a down-converted output signal 312. More specifically, in an embodiment, switch 308 closes on a first edge of each pulse 320 of FIG. 3D and opens on a second edge of each pulse. When the switch 308 is closed, the input signal 304 is coupled to the capacitor 310, and charge is transferred from the input signal to the capacitor 310. The charge stored during successive pulses forms down-converted output signal 312.

[0110] Exemplary waveforms are shown in FIGs. 3B-3F.

[0111] FIG. 3B illustrates an analog amplitude modulated (AM) carrier signal 314 that is an example of input signal 304. For illustrative purposes, in FIG. 3C, an analog AM carrier signal portion 316 illustrates a portion of the analog AM carrier signal 314 on an expanded time scale. The analog AM carrier signal portion 316 illustrates the analog AM carrier signal 314 from time t_0 to time t_1.

[0112] FIG. 3D illustrates an exemplary aliasing signal 318 that is an example of control signal 306. Aliasing signal 318 is on approximately the same time scale as the analog AM carrier signal portion 316. In the example shown in FIG. 3D, the aliasing signal 318 includes a train of pulses 320 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 320 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 318. The aliasing rate is determined as described below.

[0113] As noted above, the train of pulses 320 (i.e., control signal 306) control the switch 308 to alias the analog AM carrier signal 316 (i.e., input signal 304) at the aliasing rate of the aliasing signal 318. Specifically, in this embodiment, the switch 308 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 308 is closed, input signal 304 is coupled to the capacitor 310, and charge is transferred from the input signal 304 to the capacitor 310. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 322 form down-converted signal portion 324 (FIG. 3E) that corresponds to the analog AM carrier signal portion 316 (FIG. 3C) and the train of pulses 320 (FIG. 3D). The charge stored during successive under-samples of AM carrier signal 314 form the down-converted signal 324 (FIG. 3E) that is an example of down-converted output signal 312 (FIG. 3A). In FIG. 3F, a demodulated baseband signal 326 represents the demodulated baseband signal 324 after filtering on a compressed time scale. As illustrated, down-converted signal 326 has substantially the same

"amplitude envelope" as AM carrier signal 314. Therefore, FIGs. 3B-3F illustrate down-conversion of AM carrier signal 314.

[0114] The waveforms shown in FIGs. 3B-3F are discussed herein for illustrative purposes only, and are not limiting.

[0115] The aliasing rate of control signal 306 determines whether the input signal 304 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 304, the aliasing rate of the control signal 306, and the down-converted output signal 312 are illustrated below:

(Freq. of input signal 304) = n • (Freq. of control signal 306) ±
(Freq. of down-converted output signal 312)

[0116] For the examples contained herein, only the "+" condition will be discussed. Example values of n include, but are not limited to, n = {0.5, 1, 2, 3, 4, . . .}.

[0117] When the aliasing rate of control signal 306 is off-set from the frequency of input signal 304, or off-set from a harmonic or sub-harmonic thereof, input signal 304 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 304. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 304 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 306 would be calculated as follows:

$(Freq_{input} - Freq_{IF})/n = Freq_{control}$
(901 MHZ - 1 MHZ)/n = 900/n

[0118] For n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

[0119] Alternatively, when the aliasing rate of the control signal 306 is substantially equal to the frequency of the input signal 304, or substantially equal to a harmonic or sub-harmonic thereof, input signal 304 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal 304. As a result, the under-samples form a constant output baseband signal. If the input signal 304 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 306 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$

$$(900\ MHZ - 0\ MHZ)/n = 900\ MHZ/n$$

[0120] For n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

[0121] Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 306 would be calculated as follows:

Frequency of the input $= (F_1 + F_2) \div 2$

$= (899 \text{ MHZ} + 901 \text{ MHZ}) \div 2$

$= 900 \text{ MHZ}$

Frequency of the down-converted signal = 0 (i.e., baseband)

$(Freq_{input} - Freq_{IF})/n = Freq_{control}$

$(900 \text{ MHZ} - 0 \text{ MHZ})/n = 900 \text{ MHZ}/n$

[0122] For n = {0.5, 1, 2, 3, 4 . . .}, the frequency of the control signal 306 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

[0123] As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 306 should be substantially equal to:

(900 MHZ - 0 MHZ)/n = 900 MHZ/n, or

(901 MHZ - 0 MHZ)/n = 901 MHZ/n.

[0124] For the former case of 900 MHZ/n, and for n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

[0125] In an embodiment, the pulses of the control signal 306 have negligible apertures that tend towards zero. This makes the UFT module 302 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

[0126] In another embodiment, the pulses of the control signal 306 have non-negligible apertures that tend away from zero. This makes the UFT module 302 a lower input impedance device. This allows the lower input impedance of the UFT module 302 to be substantially matched with a source impedance of the input signal 304. This also improves the energy transfer from the input signal 304 to the down-converted output signal 312, and hence the efficiency and signal to noise (s/n) ratio of UFT module 302.

[0127] Exemplary systems and methods for generating and optimizing the control signal 306, and for otherwise improving energy transfer and s/n ratio, are disclosed in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals."

[0128] When the pulses of the control signal 306 have non-negligible apertures, the aliasing module 300 is referred to interchangeably herein as an energy transfer module or a gated transfer module, and the control signal 306 is referred to as an energy transfer signal. Exemplary systems and methods for generating and optimizing the control signal 306 and for otherwise improving energy transfer and/or signal to noise ratio in an energy transfer module are described below.

2.2 Optional Energy Transfer Signal Module

[0129] FIG. 4 illustrates an energy transfer system 401 that includes an optional energy transfer signal module 408, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal 406.

[0130] In an embodiment, the optional energy transfer signal module 408 includes an aperture generator, an example of which is illustrated in FIG. 5 as

an aperture generator 502. The aperture generator 502 generates non-negligible aperture pulses 508 from an input signal 412. The input signal 412 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal 412 are described below.

[0131] The width or aperture of the pulses 508 is determined by delay through the branch 506 of the aperture generator 502. Generally, as the desired pulse width increases, the difficulty in meeting the requirements of the aperture generator 502 decrease (i.e., the aperture generator is easier to implement). In other words, to generate non-negligible aperture pulses for a given EM input frequency, the components utilized in the example aperture generator 502 do not require reaction times as fast as those that are required in an under-sampling system operating with the same EM input frequency.

[0132] The example logic and implementation shown in the aperture generator 502 are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator 502 includes an optional inverter 510, which is shown for polarity consistency with other examples provided herein.

[0133] An example implementation of the aperture generator 502 is illustrated in FIG. 6A. Additional examples of aperture generation logic are provided in FIGs. 7A and 7B. FIG. 7A illustrates a rising edge pulse generator 702, which generates pulses 508 on rising edges of the input signal 412. FIG. 7B illustrates a falling edge pulse generator 704, which generates pulses 508 on falling edges of the input signal 412. These circuits are provided for example only, and do not limit the invention.

[0134] In an embodiment, the input signal 412 is generated externally of the energy transfer signal module 408, as illustrated in FIG. 4. Alternatively, the input signal 412 is generated internally by the energy transfer signal module 408. The input signal 412 can be generated by an oscillator, as illustrated in FIG. 6B by an oscillator 602. The oscillator 602 can be internal to the energy transfer signal module 408 or external to the energy transfer signal module

408. The oscillator 602 can be external to the energy transfer system 401. The output of the oscillator 602 may be any periodic waveform.

[0135] The type of down-conversion performed by the energy transfer system 401 depends upon the aliasing rate of the energy transfer signal 406, which is determined by the frequency of the pulses 508. The frequency of the pulses 508 is determined by the frequency of the input signal 412.

[0136] The optional energy transfer signal module 408 can be implemented in hardware, software, firmware, or any combination thereof.

2.3 Impedance Matching

[0137] The example energy transfer module 300 described in reference to FIG. 3A, above, has input and output impedances generally defined by (1) the duty cycle of the switch module (i.e., UFT 302), and (2) the impedance of the storage module (e.g., capacitor 310), at the frequencies of interest (e.g. at the EM input, and intermediate/baseband frequencies).

[0138] Starting with an aperture width of approximately ½ the period of the EM signal being down-converted as an example embodiment, this aperture width (e.g. the "closed time") can be decreased (or increased). As the aperture width is decreased, the characteristic impedance at the input and the output of the energy transfer module increases. Alternatively, as the aperture width increases from ½ the period of the EM signal being down-converted, the impedance of the energy transfer module decreases.

[0139] One of the steps in determining the characteristic input impedance of the energy transfer module could be to measure its value. In an embodiment, the energy transfer module's characteristic input impedance is 300 ohms. An impedance matching circuit can be utilized to efficiently couple an input EM signal that has a source impedance of, for example, 50 ohms, with the energy transfer module's impedance of, for example, 300 ohms. Matching these impedances can be accomplished in various manners, including providing the

necessary impedance directly or the use of an impedance match circuit as described below.

[0140] Referring to FIG. 8, a specific example embodiment using an RF signal as an input, assuming that the impedance 812 is a relatively low impedance of approximately 50 Ohms, for example, and the input impedance 816 is approximately 300 Ohms, an initial configuration for the input impedance match module 806 can include an inductor 906 and a capacitor 908, configured as shown in FIG. 9. The configuration of the inductor 906 and the capacitor 908 is a possible configuration when going from a low impedance to a high impedance. Inductor 906 and the capacitor 908 constitute an L match, the calculation of the values which is well known to those skilled in the relevant arts.

[0141] The output characteristic impedance can be impedance matched to take into consideration the desired output frequencies. One of the steps in determining the characteristic output impedance of the energy transfer module could be to measure its value. Balancing the very low impedance of the storage module at the input EM frequency, the storage module should have an impedance at the desired output frequencies that is preferably greater than or equal to the load that is intended to be driven (for example, in an embodiment, storage module impedance at a desired 1MHz output frequency is 2K ohm and the desired load to be driven is 50 ohms). An additional benefit of impedance matching is that filtering of unwanted signals can also be accomplished with the same components.

[0142] In an embodiment, the energy transfer module's characteristic output impedance is 2K ohms. An impedance matching circuit can be utilized to efficiently couple the down-converted signal with an output impedance of, for example, 2K ohms, to a load of, for example, 50 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary load impedance directly or the use of an impedance match circuit as described below.

[0143] When matching from a high impedance to a low impedance, a capacitor 914 and an inductor 916 can be configured as shown in FIG. 9. The capacitor 914 and the inductor 916 constitute an L match, the calculation of the component values being well known to those skilled in the relevant arts.

[0144] The configuration of the input impedance match module 806 and the output impedance match module 808 are considered in embodiments to be initial starting points for impedance matching, in accordance with embodiments of the present invention. In some situations, the initial designs may be suitable without further optimization. In other situations, the initial designs can be enhanced in accordance with other various design criteria and considerations.

[0145] As other optional optimizing structures and/or components are utilized, their affect on the characteristic impedance of the energy transfer module should be taken into account in the match along with their own original criteria.

2.4 Frequency Up-Conversion

[0146] The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

[0147] An example frequency up-conversion system 1000 is illustrated in FIG. 10. The frequency up-conversion system 1000 is now described.

[0148] An input signal 1002 (designated as "Control Signal" in FIG. 10) is accepted by a switch module 1004. For purposes of example only, assume that the input signal 1002 is a FM input signal 1306, an example of which is shown in FIG. 13C. FM input signal 1306 may have been generated by modulating information signal 1302 onto oscillating signal 1304 (FIGs. 13A and 13B). It should be understood that the invention is not limited to this embodiment. The information signal 1302 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

[0149] The output of switch module 1004 is a harmonically rich signal 1006, shown for example in FIG. 13D as a harmonically rich signal 1308. The harmonically rich signal 1308 has a continuous and periodic waveform.

[0150] FIG. 13E is an expanded view of two sections of harmonically rich signal 1308, section 1310 and section 1312. The harmonically rich signal 1308 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

[0151] Harmonically rich signal 1308 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 1308. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 13F and FIG. 13G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 1310 and section 1312. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 1308 is shown as a square wave, there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 13H.

[0152] The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 1006 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 1006. According to an embodiment of the invention, the input signal 1306 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

[0153] An optional filter 1008 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired

harmonic frequency or frequencies as an output signal 1010, shown for example as a filtered output signal 1314 in FIG. 13I.

[0154] FIG. 11 illustrates an example universal frequency up-conversion (UFU) module 1101. The UFU module 1101 includes an example switch module 1004, which comprises a bias signal 1102, a resistor or impedance 1104, a universal frequency translator (UFT) 1150, and a ground 1108. The UFT 1150 includes a switch 1106. The input signal 1002 (designated as "Control Signal" in FIG. 11) controls the switch 1106 in the UFT 1150, and causes it to close and open. Harmonically rich signal 1006 is generated at a node 1105 located between the resistor or impedance 1104 and the switch 1106.

[0155] Also in FIG. 11, it can be seen that an example optional filter 1008 is comprised of a capacitor 1110 and an inductor 1112 shunted to a ground 1114. The filter is designed to filter out the undesired harmonics of harmonically rich signal 1006.

[0156] The invention is not limited to the UFU embodiment shown in FIG. 11.

[0157] For example, in an alternate embodiment shown in FIG. 12, an unshaped input signal 1201 is routed to a pulse shaping module 1202. The pulse shaping module 1202 modifies the unshaped input signal 1201 to generate a (modified) input signal 1002 (designated as the "Control Signal" in FIG. 12). The input signal 1002 is routed to the switch module 1004, which operates in the manner described above. Also, the filter 1008 of FIG. 12 operates in the manner described above.

[0158] The purpose of the pulse shaping module 1202 is to define the pulse width of the input signal 1002. Recall that the input signal 1002 controls the opening and closing of the switch 1106 in switch module 1004. During such operation, the pulse width of the input signal 1002 establishes the pulse width of the harmonically rich signal 1006. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 1006 are a function of at least the pulse width of the harmonically rich signal 1006. As such, the pulse width

of the input signal 1002 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 1006.

[0159] Further details of up-conversion as described in this section are presented in U.S. Patent No. 6,091,940, entitled "Method and System for Frequency Up-Conversion," incorporated herein by reference in its entirety.

2.5 Enhanced Signal Reception

[0160] The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same, which are described in the above-referenced U.S. Patent No. 6,061,555, entitled "Method and System for Ensuring Reception of a Communications Signal," incorporated herein by reference in its entirety.

2.6 Unified Down-Conversion and Filtering

[0161] The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

[0162] In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

[0163] FIG. 14 is a conceptual block diagram of a UDF module 1402 according to an embodiment of the present invention. The UDF module 1402 performs at least frequency translation and frequency selectivity.

[0164] The effect achieved by the UDF module 1402 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1402 effectively performs input filtering.

[0165] According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

[0166] In embodiments of the invention, input signals 1404 received by the UDF module 1402 are at radio frequencies. The UDF module 1402 effectively operates to input filter these RF input signals 1404. Specifically, in these embodiments, the UDF module 1402 effectively performs input, channel select filtering of the RF input signal 1404. Accordingly, the invention achieves high selectivity at high frequencies.

[0167] The UDF module 1402 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

[0168] Conceptually, the UDF module 1402 includes a frequency translator 1408. The frequency translator 1408 conceptually represents that portion of the UDF module 1402 that performs frequency translation (down conversion).

[0169] The UDF module 1402 also conceptually includes an apparent input filter 1406 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1406 represents that portion of the UDF module 1402 that performs input filtering.

[0170] In practice, the input filtering operation performed by the UDF module 1402 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency

translation operation. This is a reason why the input filter 1406 is herein referred to as an "apparent" input filter 1406.

[0171] The UDF module 1402 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1402. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1402 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

[0172] It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

[0173] The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module 1402 can be electrically adjusted, either statically or dynamically.

[0174] Also, the UDF module 1402 can be designed to amplify input signals.

[0175] Further, the UDF module 1402 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1402 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1402 is friendly to integrated circuit design techniques and processes.

[0176] The features and advantages exhibited by the UDF module 1402 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1402 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to

frequency translation also contribute to the performance of frequency selectivity, and vice versa.

[0177] According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and/or samples/instances of the output signal.

[0178] More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

[0179] As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

[0180] Next, the input sample is held (that is, delayed).

[0181] Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

[0182] Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module 1402 preferably performs input filtering and frequency down-conversion in a unified manner.

[0183] Further details of unified down-conversion and filtering as described in this section are presented in U.S. Patent No. 6,049,706, entitled "Integrated Frequency Translation And Selectivity," filed October 21, 1998, and incorporated herein by reference in its entirety.

3. Example Embodiments of the Invention

[0184] As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications and combinations in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications and combinations.

[0185] Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals. Example receiver, transmitter, and transceiver embodiments implemented using the UFT module of the present invention are set forth below.

3.1 Receiver Embodiments

[0186] In embodiments, a receiver according to the invention includes an aliasing module for down-conversion that uses a universal frequency translation (UFT) module to down-convert an EM input signal. For example, in embodiments, the receiver includes the aliasing module 300 described above, in reference to FIG. 3A or FIG. 3G. As described in more detail above, the aliasing module 300 may be used to down-convert an EM input signal to an intermediate frequency (IF) signal or a demodulated baseband signal.

[0187] In alternate embodiments, the receiver may include the energy transfer system 401, including energy transfer module 404, described above, in reference to FIG. 4. As described in more detail above, the energy transfer system 401 may be used to down-convert an EM signal to an intermediate frequency (IF) signal or a demodulated baseband signal. As also described above, the aliasing module 300 or the energy transfer system 401 may include

an optional energy transfer signal module 408, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal 406 of various aperture widths.

[0188] In further embodiments of the present invention, the receiver may include the impedance matching circuits and/or techniques described herein for enhancing the energy transfer system of the receiver.

3.1.1 In-Phase/Quadrature-Phase (I/Q) Modulation Mode Receiver Embodiments

[0189] FIG. 15 illustrates an exemplary I/Q modulation mode embodiment of a receiver 1502, according to an embodiment of the present invention. This I/Q modulation mode embodiment is described herein for purposes of illustration, and not limitation. Alternate I/Q modulation mode embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0190] Receiver 1502 comprises an I/Q modulation mode receiver 1538, a first optional amplifier 1516, a first optional filter 1518, a second optional amplifier 1520, and a second optional filter 1522.

[0191] I/Q modulation mode receiver 1538 comprises an oscillator 1506, a first UFD module 1508, a second UFD module 1510, a first UFT module 1512, a second UFT module 1514, and a phase shifter 1524.

[0192] Oscillator 1506 provides an oscillating signal used by both first UFD module 1508 and second UFD module 1510 via the phase shifter 1524. Oscillator 1506 generates an "I" oscillating signal 1526.

[0193] "I" oscillating signal 1526 is input to first UFD module 1508. First UFD module 1508 comprises at least one UFT module 1512. First UFD

module 1508 frequency down-converts and demodulates received signal 1504 to down-converted "I" signal 1530 according to "I" oscillating signal 1526.

[0194] Phase shifter 1524 receives "I" oscillating signal 1526, and outputs "Q" oscillating signal 1528, which is a replica of "I" oscillating signal 1526 shifted preferably by 90 degrees.

[0195] Second UFD module 1510 inputs "Q" oscillating signal 1528. Second UFD module 1510 comprises at least one UFT module 1514. Second UFD module 1510 frequency down-converts and demodulates received signal 1504 to down-converted "Q" signal 1532 according to "Q" oscillating signal 1528.

[0196] Down-converted "I" signal 1530 is optionally amplified by first optional amplifier 1516 and optionally filtered by first optional filter 1518, and a first information output signal 1534 is output.

[0197] Down-converted "Q" signal 1532 is optionally amplified by second optional amplifier 1520 and optionally filtered by second optional filter 1522, and a second information output signal 1536 is output.

[0198] In the embodiment depicted in FIG. 15, first information output signal 1534 and second information output signal 1536 comprise a down-converted baseband signal. In embodiments, first information output signal 1534 and second information output signal 1536 are individually received and processed by related system components. Alternatively, first information output signal 1534 and second information output signal 1536 are recombined into a single signal before being received and processed by related system components.

[0199] Alternate configurations for I/Q modulation mode receiver 1538 will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter 1524 is coupled between received signal 1504 and UFD module 1510, instead of the configuration described above. This and other such I/Q modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

3.1.2 Receiver Embodiments Having Two Aliasing Modules

[0200] As described herein, certain receiver embodiments of the present invention are implemented using two or more aliasing modules 300. These embodiments are described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0201] FIG. 16A illustrates an exemplary receiver 1602 having two aliasing modules 300 (or, as generally the case herein, having energy transfer modules 404) according to an embodiment of the present invention. Receiver 1602 comprises an UFD module 1638, a first optional amplifier 1620, a first low-pass filter 1622, a second optional amplifier 1624, and a second low-pass filter 1626.

[0202] As illustrated in FIG. 16A, UFD module 1638 comprises two aliasing modules 1632 and 1634 and two impedances 1616 and 1618. Aliasing modules 1632 and 1634 are similar to the aliasing module shown in FIG 3G, whose operation is described herein. The output of aliasing module 1632 is coupled to impedance 1616 at a node 1605. The output of aliasing module 1634 is coupled to impedance 1618 at a node 1607. In an embodiment, impedances 1616 and 1618 are resistors. Impedances 1616 and 1618 are coupled together at a node 1609. A bias voltage is applied to node 1609.

[0203] Impedances 1616 and 1618 are illustrative, and not intended to limit the invention. In some embodiments, impedances 1616 and 1618 are a part of optional amplifiers 1620 and 1624, and thus there are no separate impedance devices 1616 and 1618 (see FIG. 16O). Similarly, in some embodiments, optional amplifiers 1620 and 1624 act as filters to the carrier signal riding on top of the down-converted signals 1650 and 1652, and thus there is no need to

include filters 1622 and 1626 (see FIG. 16O), as would be understood by a person skilled in the relevant arts given the description of the invention herein.

[0204] Aliasing module 1632 comprises a capacitor 1604 and a switching device 1608 controlled by an aperture generator 1612. One end of switching device 1608 is connected to node 1609, as shown in FIG. 16A.

[0205] FIG. 35 illustrates one embodiment for aperture generator 1612. In an embodiment, an input signal 1642 is provided to the input of aliasing module 1632. Input signal 1642 and an example control signal 1646 are illustrated in FIG. 16B.

[0206] An output signal 1650 of aliasing module 1632, for input signal 1642, is illustrated in FIG. 16C. In FIG. 16C, slope 1651 represents a down-converted signal. Slope 1654 represents the rate of discharge of capacitor 1604 between apertures. In some embodiments of the invention, low-pass filter 1622 is used to remove the carrier signal from the down-converted signal. Similarly, in some embodiments optional amplifier 1620 removes the carrier signal from the down-converted signal.

[0207] Aliasing module 1634 comprises a capacitor 1606 and a switching device 1610 controlled by an aperture generator 1614. One end of switching device 1610 is connected to node 1609, as shown in FIG. 16A. FIG. 35 illustrates one embodiment for aperture generator 1612. An input signal 1644 is provided to the input of aliasing module 1634. Input signal 1644 is generated in some embodiments of the invention by inverting signal 1642. Input signal 1644 and an example control signal 1648 are illustrated in FIG. 16B. As shown in FIG. 16B, the apertures of signal 1648 do not overlap the apertures of signal 1646. Note that the apertures of signals 1646 and 1648 are illustrative. Other portions of input signals 1642 and 1644 could be sampled in accordance with the invention to form a down-converted signal, which would involve using apertures other than the apertures shown in FIG. 16B, as will be understood by a person skilled in the relevant arts given the description of the invention herein.

[0208] An output signal 1652 of aliasing module 1634, for input signal 1644, is illustrated in FIG. 16D. In FIG. 16D, slope 1653 represents the down-converted signal. Slope 1655 represents the rate of discharge of capacitor 1606 between apertures. As described above, in some embodiments, low-pass filter 1626 is used to remove the carrier signal from the down-converted signal. In some embodiments, optional amplifier 1642 removes the carrier signal.

[0209] The output signal for UFD module 1638 (receiver 1602) is a differential output signal. FIGs. 16E and 16F illustrate an example differential output signal of UFD module 1638 (i.e., the sum of signals 1650 and 1652). An illustrative differential output signal for receiver 1602 is shown in FIG. 16G (i.e., the sum of signals 1670 and 1672). As illustrated by signals 1670 and 1672, embodiments of receiver 1602 can be used to receive and down-convert any communications signal. Carrier amplitude and phase changes relative to the sample aperture(s) are reflected in the output signals 1670 and 1672 as illustrated in FIG. 16G. FIG. 16G demonstrates the differential output when the input signal and aperture generator(s) are not related by an exact frequency multiple. As will be understood by a person skilled in the relevant arts, the sample aperture(s) roll over the input signal and capture different portions of the input signal. By illustrating that the aperture(s) can capture any amplitude and/or phase of an input signal, it is demonstrated that embodiments of receiver 1602 can be used to receive and down-convert any communications signal.

[0210] In an embodiment, the capacitors 1604 and 1606 are selected in accordance with the criteria described in section 4 below. In an embodiment, capacitors 1604 and 1606 are selected so that they discharge at a rate of between six percent to fifty percent between apertures of the control signals. However, different ranges apply to other embodiments, depending on the particular application, requirements, implementation, purpose, etc. The impedances 1616 and 1618 typically have similar values (e.g., impedances

1616 and 1618 may be resistors having the same nominal values but different actual values).

[0211] In an embodiment, the period of control signals 1646 and 1648 operate at a third or a fifth harmonic of the input carrier signal (i.e., input signals 1642 and 1644). In an embodiment, switching device 1608 is closed for approximately one-half cycle of the input signal 1642 each period of control signal 1646. Similarly, switching device 1610 is closed for approximately one-half cycle of the input signal 1644 each period of control signal 1648.

[0212] In an embodiment, aperture generator 1614 is coupled to a clock signal that is 180 degrees out of phase with respect to the clock signal coupled to aperture generator 1612. In an embodiment, the clock signal coupled to aperture generator 1614 has the same period as the clock signal coupled to aperture generator 1612.

[0213] The operation of receiver 1602 will now be described.

[0214] A modulated carrier signal 1642 is input to the carrier(+) port of receiver 1602. The modulated carrier signal causes a charge to be stored on capacitor 1604 when switching device 1608 is closed. Switching device 1608 is opened and closed by control signal 1646. Aperture generator 1612 generates control signal 1646.

[0215] The modulated carrier signal 1642 is inverted to generate a signal 1644. Signal 1644 is input to the carrier(-) port of receiver 1602. Signal 1644 causes a charge to be stored on capacitor 1606 when switching device 1610 is closed. Switching device 1610 is opened and closed by control signal 1648. Aperture generator 1614 generates control signal 1648.

[0216] When switching device 1608 is open, capacitor 1604 discharges. This causes a voltage signal to be generated across impedance 1616. Similarly, when switching device 1610 is open, capacitor 1606 discharges. This causes a voltage signal to be generated across impedance 1618. The opening and closing of switching devices 1608 and 1610 in accordance with the invention causes a down-converted signal 1650 (one-half of the output of receiver 1602) to be formed across impedance 1616 and a down-converted signal 1652 (one-

half of the output of receiver 1602) to be formed across impedance 1618. Signals 1650 and 1652 are 180 degrees out of phase. The total output of receiver 1602 is the differential output, or the sum of signals 1650 and 1652. Filters 1622 and 1626 are used to remove the carrier from the down-converted signal. As described herein, in embodiments, optional amplifiers 1620 and 1624 are band limited, and thus act as filters and remover the carrier.

[0217] As will be understood by a person skilled in the relevant arts, given the description of the invention herein, UFD module 1638 has several features that make it particularly well adapted for certain applications. It is a feature of UFD module 1638 that it has an impedance in a range of about 50-75 ohms for certain control signals. UFD module 1638 can thus be coupled to other circuit devices that comprise receiver 1602 without using an impedance matching circuit as described herein (although one could optionally be used). This feature of UFD module 1638 allows for a high power or energy transfer, and it minimizes or eliminates interfacing requirements. Another feature of UFD module 1638 is that it may be implemented on a single chip using CMOS technology. This feature of UFD module 1638 is a feature applicable to apparatus embodiments of the invention in general.

[0218] FIG. 16H illustrates another embodiment of a UFD module 1688 according to the invention. In the embodiment of FIG. 16H, aliasing modules of the type shown in FIG. 3A are used. This embodiment of the invention operates similarly to UFD module 1638, except that the carrier signal is removed from the down converted signal by capacitors 1604 and 1606 during down-conversion.

[0219] FIG. 16I illustrates one possible relationship between example input signals 1643 and 1645 and example control signals 1647 and 1649. As described about, the apertures of signals 1647 and 1649 are illustrative. Other portions of input signals 1643 and 1644 could be sampled in accordance with the invention to form a down-converted signal, which would involve using apertures other than the apertures shown in FIG. 16I, as will be understood by

a person skilled in the relevant arts given the description of the invention herein.

[0220] FIGs. 16J-16L illustrate down-converted signals for the receiver of FIG. 16H. FIG. 16J illustrates a down-converted signal 1651, for input signal 1643. As can be seen in FIG. 16J, down-converted signal 1651 is similar to down-converted signal 1652 (note that the carrier has not been removed from signal 1652 and is riding on top of the down-converted signal). Similarly, FIG. 16K illustrates a down-converted signal 1653, for input signal 1645. As can be seen in FIG. 16K, down-converted signal 1653 is similar to down-converted signal 1651 (note that the carrier has not been removed from signal 1651 and is riding on top of the down-converted signal). Signals 1651 and 1653 are plotted together with control signals 1647 and 1649 in FIG. 16L.

[0221] FIG. 16M illustrates the outputs of the UFD module 1688 in FIG. 16H. FIG. 16M is similar to FIG. 16F. One significant difference, however, as can be seen between FIGs. 16M and 16F, however, is that signals 1651 and 1653 do not go to zero during each period of the control signals 1647 and 1649. This is not the case for the UFD module 1638 in FIG. 16A, as can be see by looking at signals 1650 and 1652. When the switching devices 1608 and 1610, as configured in FIG. 16H, are closed, the output of UFD module 1688 is not connected to a bias point (AC ground).

[0222] FIG. 16N illustrates the filtered output of the receiver of FIG. 16H. As can be seen by comparing FIGs. 16G and 16N, the filtered outputs of the receiver embodiments shown in FIGs. 16A and 16H are the same, thereby demonstrating the interchangeability of embodiments of aliasing modules and/or energy transfer modules according to the invention in embodiments of the invention.

[0223] As illustrated by signals 1671 and 1673, in FIG. 16N, embodiments of the receiver of FIG. 16H can be used to receive and down-convert any communications signal. Carrier amplitude and phase changes relative to the sample aperture(s) are reflected in the output signals 1671 and 1673 as illustrated in FIG. 16N. FIG. 16N demonstrates the differential output when

the input signal and aperture generator(s) are not related by an exact frequency multiple. As will be understood by a person skilled in the relevant arts, the sample aperture(s) roll over the input signal and capture different portions of the input signal. By illustrating that the aperture(s) can capture any amplitude and/or phase of an input signal, it is demonstrated that embodiments of the receiver of FIG. 16H can be used to receive and down-convert any communications signal.

[0224] The operation of the receiver of FIG. 16H is similar to that of receiver 1602, and thus is not repeated here. A person skilled in the relevant art will understand how the receiver of FIG. 16H operates given the description of the invention herein.

[0225] FIG. 17 illustrates a receiver 1702 according to an embodiment of the invention having two aliasing modules. Receiver 1702 is similar to receiver 1602. Like receiver 1602, example receiver 1702 is implemented using aliasing modules similar to the embodiment shown in FIG. 3G.

[0226] Receiver 1702 comprises a UFD 1738, an inverter 1703, two optional amplifiers 1720 and 1724, and two low-pass filters 1722 and 1726. The aliasing modules of UFD 1738 are implemented using switches 1708 and 1710. In the embodiment of FIG. 17, switches 1708 and 1710 are formed using complementary enhancement type MOSFETs. A bias voltage 1711 is coupled to a node 1709 of UFD 1738.

[0227] A modulated carrier signal is supplied to one of the input ports of UFD module 1738. An inverter 1703 is used to invert the modulated carrier signal and thereby produce a carrier(-) signal. An uninverted modulated carrier signal is referred to herein as a carrier(+) signal. The output of inverter 1703 is supplied to a second input port of UFD module 1738, as shown in FIG. 17.

[0228] As will be understood by a person skilled in the relevant arts, UFD module 1738 operates in a manner similar to that described herein, for example, for UFD module 1638. The various signals of receiver 1702 are similar to the signals illustrated in FIGs. 16B-G.

[0229] The operation of receiver 1702 is also similar to that of receiver 1602, and thus is not repeated here. A person skilled in the relevant art will understand how receiver 1702 operates given the description of the invention herein.

3.1.3 Enhanced Single-Switch Receiver Embodiments

[0230] As described herein, single-switch receiver embodiments of the present invention are enhanced to maximize both power transfer and information extraction. These embodiments are described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0231] FIG. 18A illustrates an exemplary one-switch receiver 1802 according to an embodiment of the invention. Receiver 1802 comprises a UFD module 1832, a first optional amplifier 1820, a first low-pass filter 1822, a second optional amplifier 1824, and a second low-pass filter 1826.

[0232] As illustrated in FIG. 18A, UFD module 1832 comprises two capacitors 1804 and 1806, a switching device 1808, a switching signal generator 1812, and two impedance devices 1816 and 1818. In an embodiment, impedance devices 1816 and 1818 are resistors. Impedance devices 1816 and 1818 are coupled together at a node 1809. A bias voltage is applied to node 1809.

[0233] Impedances 1816 and 1818 are illustrative, and not intended to limit the invention. In some embodiment, impedances 1816 and 1818 are a part of optional amplifiers 1820 and 1824, and thus there are no separate impedance devices 1816 and 1818. Similarly, in some embodiments, optional amplifiers 1820 and 1824 act as filters to the carrier signal riding on top of the down-converted signals 1850 and 1852, and thus there is no need to include filters

1822 and 1826, as would be understood by a person skilled in the relevant arts given the description of the invention herein.

[0234] FIG. 35 illustrates one embodiment for switching device (aperture generator) 1812. An example control signal 1846 is illustrated in FIG. 18B.

[0235] FIGs. 18B-18E illustrate example waveforms for receiver 1802. The waveforms are for an embodiment of the invention wherein capacitors 1804 and 1806 have a nominal value of 11 pf and impedance devices 1816 and 1818 are resistors having a nominal value of 547 ohms. The waveforms illustrated are for a 1 GHz input carrier signal.

[0236] In an embodiment, the capacitors 1804 and 1806 are selected in accordance with the criteria described in section 4 below. Capacitors 1804 and 1806 are selected so that they discharge at a rate of between six percent to fifty percent between apertures of the switching (control) signal.

[0237] In an embodiment, the period of control signal 1846 operates at a third or a fifth harmonic of the input carrier signal (i.e., input signals 1842 and 1844). As described herein, the received carrier signal is referred to as a carrier(+) signal, and an inverted version of the received signal is referred to as a carrier(-) signal. Switching device 1808 is closed for approximately one-half cycle of the input signal 1842 each period of control signal 1846.

[0238] FIG. 18B illustrates a switching signal (aperture generator signal) 1846. Also shown in FIG. 18B is a voltage signal 1860 across capacitor 1804, and a voltage signal 1862 across capacitor 1806. The voltage across capacitors 1804 and 1806 increases when switch 1808 is closed. The voltage across capacitors 1804 and 1806 decreases when switch 1808 is open. Slope 1861 in FIG. 18B illustrates the discharge of capacitor 1806 between the apertures of switching (control) signal 1846. A similar discharge occurs for capacitor 1804, as can be seen from signal 1860.

[0239] FIG. 18C illustrates the output(+) signal 1850 of UFD module 1832 and the output(-) signal 1852 of UFD module 1832. These signals contain both a down-converted (information) signal and the carrier signal. Switching signal 1842 is also shown as a point of reference. Slope 1851 in FIG. 18C is

due to the discharge of capacitor 1804, and illustrates that energy is being transferred in accordance with the invention.

[0240] FIG. 18D illustrates the output signal of UFD module 1832 after the carrier signal has been removed using low-pass filters 1822 and 1826. Signal 1870 shows the output of filter 1822. Signal 1872 shows the output of filter 1826. Switching signal 1846 is shown in FIG. 18D for reference.

[0241] FIG. 18E shows the output of receiver 1802 for an extended period of time, as illustrated by switching signal 1846. In FIG. 18E, the input carrier signal has a frequency of 1 GHz, but the period of switching signal 1846 has been extended from 3.000 ns (as is the case for the waveforms of FIGs. 18B-D) to 3.003 ns. Thus, the phase of the input carrier signal is slowly varying relative to switching signal 1846. Signal 1870 in FIG. 18E is the output of filter 1822. Signal 1872 is the output of filter 1826.

[0242] As illustrated by signals 1870 and 1872, embodiments of receiver 1802 can be used to receive and down-convert any communications signal. Carrier amplitude and phase changes relative to the sample aperture(s) are reflected in the output signals 1870 and 1872 as illustrated in FIG. 18E. FIG. 18E demonstrates the differential output when the input signal and aperture generator are not related by an exact frequency multiple. As will be understood by a person skilled in the relevant arts, the sample aperture(s) roll over the input signal and capture different portions of the input signal. By illustrating that the aperture(s) can capture any amplitude and/or phase of an input signal, it is demonstrated that embodiments of receiver 1802 can be used to receive and down-convert any communications signal.

[0243] The operation of receiver 1802 will now be described.

[0244] A modulated carrier signal 1642 is input to the carrier(+) port of receiver 1802. The modulated carrier signal causes a charge to be stored on capacitor 1804 when switching device 1808 is closed, thereby generating a voltage signal 1860 across capacitor 1804. Switching device 1808 is opened and closed by control signal 1846. Aperture generator 1812 generates control signal 1846.

[0245] The modulated carrier signal 1642 is inverted to generate a signal 1644. Signal 1644 is input to the carrier(-) port of receiver 1802. Signal 1644 causes a charge to be stored on capacitor 1806 when switching device 1808 is closed, thereby generating a voltage signal 1862 across capacitor 1806.

[0246] When switching device 1808 is opened, both capacitor 1804 and capacitor 1806 begin to discharge. This causes a voltage signal 1850 to be generated across impedance 1816, and a voltage signal 1852 to be generated across impedance 1818.

[0247] The opening and closing of switching device 1808 in accordance with the invention causes a down-converted signal 1850 (one-half of the output of receiver 1802) to be formed across impedance 1816 and a down-converted signal 1852 (one-half of the output of receiver 1802) to be formed across impedance 1818. Signals 1850 and 1852 are 180 degrees out of phase. The total output of receiver 1802 is the differential output, or the sum of signals 1850 and 1852. Filters 1822 and 1826 are used to remove the carrier from the down-converted signal. In embodiments, optional amplifiers 1820 and 1824 are band limited, and thus act as filters and remover the carrier.

[0248] As will be understood by a person skilled in the relevant arts, given the description of the invention herein, UFD module 1832 has several features that make it particularly well adapted for certain applications. It is a feature of UFD module 1832 that it provides exceptional linearity per milliwatt. For example, rail to rail dynamic range is possible with minimal increase in power. In an example integrated circuit embodiment, UFD module 1832 provides +55dmb IP2, +15 dbm IP3, at 3.3V, 4.4ma, -15dmb LO. GSM system requirements are +22dbm IP2, -10.5dmb IP3. CDMA system requirements are +50dmb IP2, +10dbm IP3. Accordingly, the invention satisfies these standards. Another feature of UFD module 1832 is that it only requires one switching device 1808 and one aperture generator 1812. A further feature of UFD module 1832 is that it may be implemented on a single chip using CMOS technology. As described herein, this feature of UFD module 1832 is

a feature applicable to apparatus embodiments of the invention in general. Additional features of UFD module 1832 are described elsewhere herein.

[0249] FIG. 19 is another example of a one-switch receiver 1902 having a UFD module 1938 according to an embodiment of the invention. As illustrated in FIG. 19, UFD module 1938 comprises two capacitors 1904 and 1906, a CMOS switching device 1908, two switching signal generators 1912A and 1912B, and two impedance devices 1916 and 1918. In an embodiment, impedance devices 1916 and 1918 are resistors. Impedance devices 1916 and 1918 are coupled together at a node 1909. A bias voltage 1911 (AC Ground) having a nominal value of one-half Vdd is applied to node 1909. As illustrated in FIG. 19, in an embodiment, a transformer 1960 is used to couple an input signal to UFD module 1938.

[0250] As already described herein, impedances 1916 and 1918 are illustrative, and not intended to limit the invention. In some embodiment, impedances 1916 and 1918 are a part of optional amplifiers (not shown), and thus there are no separate impedance devices 1916 and 1918. Similarly, in some embodiments, optional amplifiers (not shown) act as filters to the carrier signal riding on top of the down-converted signals, and thus there is no need to include filters with receiver 1902.

[0251] As will be understood by a person skilled in the relevant arts, UFD module 1938 operates in a manner similar to that described herein, for example, for UFD module 1832. Features of UFD module 1938 are also described below in section 4. In particular, the enhanced linear features of UFD module 1938 are described in detail below.

[0252] The operation of receiver 1902 is similar to that of receiver 1802, and thus is not repeated here. A person skilled in the relevant art will understand how receiver 1902 operates given the description of the invention herein.

[0253] FIG. 20A is an example one-switch receiver 2001 having an aliasing module 2032 according to an embodiment of the invention and an impedance device 2016. Aliasing module 2032 is of the type illustrated in FIG. 3G. Impedance 2016 is illustrative, and not intended to limit the invention. In

some embodiment, impedance 2016 is a part of an optional amplifier (not shown), and thus there is no separate impedance device 2016.

[0254] As illustrated in FIG. 20A, UFD module 2032 comprises a capacitor 2004, a switching device 2008 and an aperture generator 2012. Impedance device 2016 is coupled to switching device 2008, as shown in FIG. 20A. A bias voltage (AC ground) is applied to a node 2009. As will be apparent to a person skilled in the relevant arts, generally speaking, receiver 2001 comprises one-half of receiver 1602.

[0255] In an embodiment, capacitor 2004 is selected in accordance with the criteria described in section 4 below. Capacitor 2004 is selected so that it discharges at a rate of between six percent to fifty percent between apertures of switching (control) signal 2046. The period of control signal 2046 operates at a third or a fifth harmonic of the input carrier signal. Switching device 2008 is closed for approximately one-half cycle of the input signal during each period of control signal 2046.

[0256] FIGs. 20B-20D illustrate example waveforms for receiver 2001. The waveforms are for an embodiment of the invention, wherein capacitor 2004 has a nominal value of 11 pf and impedance device 2016 is resistor having a nominal value of 547 ohms. The waveforms illustrated are for a 1 GHz input carrier signal.

[0257] FIG. 20B illustrates a switching signal (aperture generator signal) 2046. Also shown in FIG. 208B is a voltage signal 2060 across capacitor 2004. The voltage across capacitor 2004 increases when switch 2008 is closed. The voltage across capacitor 2004 decreases when switch 2008 is open. A periodic slope in signal 2060 illustrates the discharge of capacitor 2004 between the apertures of switching (control) signal 2046. Signal 2050 illustrates the output of receiver 2001. As can be seen, the output comprises both a down-converter signal and the carrier. The carrier can be removed using a filter (not shown).

[0258] FIG. 20C illustrates the output signal 2070 of UFD module 2032 after the carrier signal has been removed. Switching signal 2046 is shown in FIG. 20C for reference.

[0259] FIG. 20D shows the output of receiver 2001 for an extended period of time, as illustrated by switching signal 2046. In FIG. 20D, the input carrier signal has a frequency of 1 GHz, but the period of switching signal 2046 has been extended from 3.000 ns (as is the case for the waveforms of FIGs. 20B-20C) to 3.003 ns. Thus, the phase of the input carrier signal is slowly varying relative to switching signal 2046. Signal 2070 in FIG. 20D is the output of UFD module 2032 after the carrier has been removed by low-pass filtering.

[0260] As illustrated by signal 1870, in FIG. 29D, embodiments of receiver 2001 can be used to receive and down-convert any communications signal. Carrier amplitude and phase changes relative to the sample aperture(s) are reflected in the output signal 2070 as illustrated in FIG. 20D. FIG. 20D demonstrates the output when the input signal and aperture generator are not related by an exact frequency multiple. As will be understood by a person skilled in the relevant arts, the sample aperture(s) roll over the input signal and capture different portions of the input signal. By illustrating that the aperture(s) can capture any amplitude and/or phase of an input signal, it is demonstrated that embodiments of receiver 2001 can be used to receive and down-convert any communications signal.

[0261] The operation of receiver 2001 is similar to that of other receiver embodiments already described herein. A modulated carrier signal is input to the carrier port of receiver 2101. The modulated carrier signal causes a charge to be stored on capacitor 2104 and capacitor 2106 when switching device 2108 is closed, thereby generating a voltage signal across capacitors 2104 and 2106. Switching device 2108 is opened and closed by control signal having apertures similar to other control signals illustrated herein. Aperture generator 2112 generates the control signal.

[0262] A difference between receiver 2101 and receiver 1802, for example, is that the modulated carrier signal is not inverted to input to a carrier(-) port. As

can be seen in FIG. 21, the second input port of receiver 2101 is coupled to a ground.

[0263] When switching device 2108 is opened, both capacitor 2104 and capacitor 2106 begin to discharge. This causes a voltage to be generated across impedance 2116, and a voltage to be generated across impedance 2118.

[0264] The opening and closing of switching device 2108 in accordance with the invention causes a down-converted signal (one-half of the output of receiver 2101) to be formed across impedance 2116 and a down-converted signal (one-half of the output of receiver 2101) to be formed across impedance 2118. The total output of receiver 2101 is the differential output, or the sum of signals. Filters (not shown) are used to remove the carrier from the down-converted signal. In embodiments, optional amplifiers (not shown) are band limited, and thus act as filters and remover the carrier.

[0265] As will be understood by a person skilled in the relevant arts, given the description of the invention herein, receiver 2001 has several features that make it particularly well adapted for certain applications. For example, it is a feature of receiver 2001 that it may be implemented using fewer devices than other embodiments and that it may be implemented on a single chip using CMOS technology.

[0266] FIG. 20E illustrates a signal switch receiver 2002 having an aliasing module 2032 according to an embodiment of the invention and an impedance device 2016. Aliasing module 2032 is of the type illustrated in FIG. 3G.

[0267] As illustrated in FIG. 20E, UFD module 2032 comprises a capacitor 2004, a switching device 2008 and two aperture generators 2012A and 2012B. Impedance device 2016 is coupled to switching device 2008, as shown in FIG. 20A. A bias voltage (AC ground) is applied to a node 2009. Receiver 2002 is similar to receiver 2001.

[0268] The operation of receiver 2002 is similar to that of other receiver embodiments already described herein, and thus is not repeated here. A person skilled in the relevant art will understand how receiver 2001 operates given the description of the invention herein.

[0269] FIG. 20F illustrates another embodiment of a single switch receiver 2003 having an aliasing module 2032 according to the invention. In the embodiment of FIG. 20F, an aliasing module of the type shown in FIG. 3A is used. This embodiment of the invention operates similarly to receiver 2001, except that the carrier signal is removed from the down converted signal by capacitor 2004 during down-conversion.

[0270] Since the operation of receiver 2003 is similar to that of other receiver embodiments already described herein, it is not repeated here. A person skilled in the relevant art will understand how receiver 2003 operates given the description of the invention herein.

[0271] FIG. 21 is another example one-switch receiver 2101 according to an embodiment of the invention. Receiver 2101 comprises a UFD module 2138, similar to UFD module 1832, described above. As seen in FIG. 21, one of the input ports of UFD module 2138 is coupled to ground. It is a feature of receiver 2101 that no carrier(-) input signal is required. The operation of receiver 2101 is similar to that of other receiver embodiments already described herein, and thus is not repeated here. A person skilled in the relevant art will understand how receiver 2101 operates given the description of the invention herein.

3.1.4 Other Receiver Embodiments

[0272] The receiver embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments include, but are not limited to, down-converting different combinations of modulation techniques in an "I/Q" mode. Other embodiments include those shown in the documents referenced above, including but not limited to U.S. Patent

Application Ser. Nos. 09/525,615 and 09/550,644. Such alternate embodiments fall within the scope and spirit of the present invention.

[0273] For example, other receiver embodiments may down-convert signals that have been modulated with other modulation techniques. These would be apparent to one skilled in the relevant art(s) based on the teachings disclosed herein, and include, but are not limited to, amplitude modulation (AM), frequency modulation (FM), pulse width modulation, quadrature amplitude modulation (QAM), quadrature phase-shift keying (QPSK), time division multiple access (TDMA), frequency division multiple access (FDMA), code division multiple access (CDMA), down-converting a signal with two forms of modulation embedding thereon, and combinations thereof.

3.2 Transmitter Embodiments

[0274] The following discussion describes frequency up-converting signals transmitted according to the present invention, using a Universal Frequency Up-conversion Module. Frequency up-conversion of an EM signal is described above, and is more fully described in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998 and issued July 18, 2000, the full disclosure of which is incorporated herein by reference in its entirety, as well as in the other documents referenced above (see, for example, U.S. Patent Application Ser. No. 09/525,615).

[0275] Exemplary embodiments of a transmitter according to the invention are described below. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0276] In embodiments, the transmitter includes a universal frequency up-conversion (UFU) module for frequency up-converting an input signal. For example, in embodiments, the system transmitter includes the UFU module

1000, the UFU module 1101, or the UFU module 1290 as described, above, in reference to FIGs. 10, 11 and 12, respectively. In further embodiments, the UFU module is used to both modulate and up-convert an input signal.

3.2.1 In-Phase/Quadrature-Phase (I/Q) Modulation Mode Transmitter Embodiments

[0277] In FIG. 22, an I/Q modulation mode transmitter embodiment is presented. In this embodiment, two information signals are accepted. An in-phase signal ("I") is modulated such that its phase varies as a function of one of the information signals, and a quadrature-phase signal ("Q") is modulated such that its phase varies as a function of the other information signal. The two modulated signals are combined to form an "I/Q" modulated signal and transmitted. In this manner, for instance, two separate information signals could be transmitted in a single signal simultaneously. Other uses for this type of modulation would be apparent to persons skilled in the relevant art(s).

[0278] FIG. 22 illustrates an exemplary block diagram of a transmitter 2202 in an I/Q modulation mode. In FIG. 22, a baseband signal comprises two signals, first information signal 2212 and second information signal 2214. Transmitter 2202 comprises an I/Q transmitter 2204 and an optional amplifier 2206. I/Q transmitter 2204 comprises at least one UFT module 2210. I/Q transmitter 2204 provides I/Q modulation to first information signal 2212 and second information signal 2214, outputting I/Q output signal 2216. Optional amplifier 2206 optionally amplifies I/Q output signal 2216, outputting up-converted signal 2218.

[0279] FIG. 23 illustrates a more detailed circuit block diagram for I/Q transmitter 2204. I/Q transmitter 2204 is described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings

contained herein. The invention is intended and adapted to include such alternate embodiments.

[0280] I/Q transmitter 2204 comprises a first UFU module 2302, a second UFU module 2304, an oscillator 2306, a phase shifter 2308, a summer 2310, a first UFT module 2312, a second UFT module 2314, a first phase modulator 2328, and a second phase modulator 2330.

[0281] Oscillator 2306 generates an "I"-oscillating signal 2316.

[0282] A first information signal 2212 is input to first phase modulator 2328. The "I"-oscillating signal 2316 is modulated by first information signal 2212 in the first phase modulator 2328, thereby producing an "I"-modulated signal 2320.

[0283] First UFU module 2302 inputs "I"-modulated signal 2320, and generates a harmonically rich "I" signal 2324 with a continuous and periodic wave form.

[0284] The phase of "I"-oscillating signal 2316 is shifted by phase shifter 2308 to create "Q"-oscillating signal 2318. Phase shifter 2308 preferably shifts the phase of "I"-oscillating signal 2316 by 90 degrees.

[0285] A second information signal 2214 is input to second phase modulator 2330. "Q"-oscillating signal 2318 is modulated by second information signal 2214 in second phase modulator 2330, thereby producing a "Q" modulated signal 2322.

[0286] Second UFU module 2304 inputs "Q" modulated signal 2322, and generates a harmonically rich "Q" signal 2326, with a continuous and periodic waveform.

[0287] Harmonically rich "I" signal 2324 and harmonically rich "Q" signal 2326 are preferably rectangular waves, such as square waves or pulses (although the invention is not limited to this embodiment), and are comprised of pluralities of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveforms. These sinusoidal waves are referred to as the harmonics of the underlying waveforms, and a Fourier analysis will determine the amplitude of each harmonic.

[0288] Harmonically rich "I" signal 2324 and harmonically rich "Q" signal 2326 are combined by summer 2310 to create harmonically rich "I/Q" signal 2334. Summers are well known to persons skilled in the relevant art(s).

[0289] Optional filter 2332 filters out the undesired harmonic frequencies, and outputs an I/Q output signal 2216 at the desired harmonic frequency or frequencies.

[0290] It will be apparent to persons skilled in the relevant art(s) that an alternative embodiment exists wherein the harmonically rich "I" signal 2324 and the harmonically rich "Q" signal 2326 may be filtered before they are summed, and further, another alternative embodiment exists wherein "I"-modulated signal 2320 and "Q"-modulated signal 2322 may be summed to create an "I/Q"-modulated signal before being routed to a switch module. Other "I/Q"-modulation embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention. Further details pertaining to an I/Q modulation mode transmitter are provided in co-pending U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," filed October 21, 1998 and issued July 18, 2000, which is incorporated herein by reference in its entirety.

3.2.2 Enhanced Multi-Switch Transmitter Embodiments

[0291] As described herein, multi-switch transmitter embodiments of the present invention are enhanced to maximize both power transfer and information transmission. These embodiments are described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0292] FIG. 24A is an example two-switch transmitter 2402 according to an embodiment of the invention. Transmitter 2402 comprises two switching devices 2408 and 2410, two aperture generators 2412 and 2414, an impedance device 2419, and two amplifiers 2432 and 2434.

[0293] As shown in FIG. 24A, amplifiers 2432 and 2434, and impedance device 2419 are coupled together to form a node 2409. Node 2409 is an AC ground. In an embodiment, impedance device 2419 is an inductor. Impedance device 2419 comprises a feedback path that passes DC signals to the inputs of amplifiers 2432 and 2434, thereby removing the DC signals from the output of transmitter 2402. The output ports of amplifiers 2432 and 2434 are coupled to switching devices 2408 and 2410. Switching devices 2408 and 2410, and impedance device 2419 are coupled together to form a node 2405. The output of transmitter 2402 is generated at node 2405, across a load impedance 2470. Load impedance 2470 is illustrative, and not intended to limit the invention.

[0294] In an embodiment, optional energy storage devices (capacitors) 2431 and 2433 are coupled to transmitter 2402, as shown in FIG. 24A, in order to increase the efficiency of transmitter 2402. Energy storage devices 2431 and 2433. These devices store energy when switches 2408 and 2410 are open, thereby enhancing the energy transmitted when switches 2408 and 2410 close. Energy storage devices 2431 and 2433 can be coupled to any bias (AC ground).

[0295] It is a feature of example transmitter 2402, as well as a feature of other embodiments of the invention, that no power summer is needed at node 2405 so long as the apertures of switching devices 2408 and 2410 do not overlap. A simple wire can be used to couple transmitter 2402 to load impedance 2470. Other approaches may also be used.

[0296] The operation of transmitter 2402 will now be described with reference to the waveforms illustrated in FIGs. 24B-24F.

[0297] An information signal 2442 to be up-converted is provided to the input(+) port of amplifier 2442 (see FIG. 24E). As shown in FIG. 24E,

information signal 2442 is a sine wave. An inverted version of information signal 2442 (i.e., signal 2444) is provided to the input(-) port of amplifier 2434. Signal 2444 is shown in FIG. 24E.

[0298] Input signals 2442 and 2444 are operated on by amplifiers 2432 and 2434 in a manner that would be known to a person skilled in the relevant art to produce signals at the outputs of amplifiers 2432 and 2434 that are a function of (i.e., proportional to) the input signals 2442 and 2444. When switch 2408 is closed, the output signal of amplifier 2432 is coupled to load impedance 2470, and thereby produces a positive voltage at the input of impedance 2470 such as, for example, voltage 2405B shown in FIG. 24C. Similarly, when switch 2410 is closed, the output signal of amplifier 2434 is coupled to load impedance 2470, and thereby produces a negative voltage at the input of impedance 2470 such as, for example, voltage 2405A shown in FIG. 24C. The operation of switching devices 2408 and 2410 are controlled by control signals 2446 and 2448. These signals are illustrated in FIGs. 24B and 24C. Control signal 2446 controls the switching of switching device 2408. Control signal 2448 controls the switching of switching device 2410.

[0299] As can be seen in FIG. 24B, the opening and closing of switching devices 2408 and 2410 produce a harmonically rich up-converted signal 2405. Up-converted signal 2405 is also illustrated in FIGs. 24D and 24E. In particular, FIG. 24E illustrates the relationship between input signals 2442 and 2444 and up-converted signal 2405.

[0300] FIG. 24F illustrates a portion of Fourier transform of up-converted signal 2405. As illustrated in FIG. 24F, signal 2405 of transmitter 2402 is a harmonically rich signal. The particular portion of signal 2405 that is to be transmitted can be selected using a filter. For example, a high Q filter centered at 1.0 GHz can be used to select the 3rd harmonic portion of signal 2405 for transmission. A person skilled in the relevant arts will understand how to do this given the description of the invention herein. In embodiments, the output signal 2405 is routed to a filter (not shown) to remove the unwanted frequencies that exist as harmonic components of the harmonically rich signal.

A desired frequency is optionally amplified by an amplifier module (not shown) and then optionally routed to a transmission module (not shown) for transmission.

[0301] As described herein, optional energy storage devices 2431 and 2433 as well as impedance matching techniques can be used to improve the efficiency of transmitter 2402.

[0302] FIGs. 24G-24K further illustrate the operation of transmitter 2402 when transmitter 2402 is used, for example, to transmit digital information represented by the input signals shown in FIGs. 24G and 24H. FIG. 24G illustrates an example digital signal 2442 that represents a bit sequence of "1011." The inverse of signal 2442 (i.e., 2444) is illustrated in FIG. 24H. Input signals 2442 and 2444 are input to amplifiers 2432 and 2434, as described above. FIG. 24I illustrates an example control 2446. FIG. 24J illustrates an example control signal 2448. A harmonically rich up-converted signal 2405, for the input signals 2442 and 2444 (shown in FIGs. 24G and 24H), is shown in FIG. 24K. Signal 2405 of FIG. 24K s obtain in the manner described above.

[0303] The example waveforms of FIGs. 24B-24K are illustrative, and not intended to limit the invention. Waveforms other than those illustrated in FIGS. 24B-24K are intended to be used with the architecture that comprises transmitter 2402.

[0304] FIG. 25A is an example two-switch transmitter 2502 according to an embodiment of the invention. Transmitter 2502 comprises two switching devices 2508 and 2510, two aperture generators 2512 and 2514, three impedance devices 2519, 2533, and 2535, and two amplifiers 2532 and 2534.

[0305] As shown in FIG. 25A, amplifiers 2532, 2534, switching devices 2508, 2510, and impedance device 2519 are coupled together to form a node 2509. Node 2509 is an AC ground. In an embodiment, impedance device 2519 is an inductor. Impedance device 2519 comprises a feedback path that passes DC signals to the inputs of amplifiers 2532 and 2534, thereby removing the DC signals from the output of transmitter 2502. The output ports of amplifiers

2532 and 2534 are coupled to impedance devices 2533 and 2535. Impedance devices 2533 and 2535 represent one or more impedance devices that act as an AC choke (low pass filter). Impedance devices 2533, 2535, switching devices 2508, 2510, and impedance device 2519 are also coupled together to form a node 2505. The output of transmitter 2502 is generated at node 2505, across a load impedance 2570.

[0306] The operation of switching devices 2508 and 2510 is controlled by control signals 2546 and 2548. Example control signals are illustrated in FIGs. 25D and 25E. Control signal 2546 controls the switching of switching device 2508. Control signal 2548 controls the switching of switching device 2510.

[0307] The operation of transmitter 2502 is similar to that of transmitter 2402, and thus is not repeated here. A person skilled in the relevant art will understand how transmitter 2502 operates given the description of the invention herein.

[0308] FIGs. 25B-25F illustrate the operation of transmitter 2502 when transmitter 2502 is used, for example, to transmit digital information represented by the input signals shown in FIGs. 25B and 25C. The example waveforms of FIGs. 25B-25F are illustrative, and not intended to limit the invention. Waveforms other than those illustrated in FIGS. 25B-25F are intended to be used with the architecture that comprises transmitter 2502.

[0309] FIG. 25B illustrates an example digital signal 2542 that represents a bit sequence of "1011." The inverse of signal 2542 (i.e., 2544) is illustrated in FIG. 25C. Input signals 2542 and 2544 are input to amplifiers 2532 and 2534. FIG. 25D illustrates an example control 2546. FIG. 25E illustrates an example control signal 2548. A harmonically rich up-converted signal 2550, for the input signals 2542 and 2544 is shown in FIG. 25F.

[0310] As described herein for transmitter 2402, optional energy storage devices (not shown) as well as impedance matching techniques can be used to improve the efficiency of transmitter 2502. How this is achieved in

accordance with will be understood by a person skilled in the relevant arts given the description herein.

[0311] FIG. 26A is example of a multi-switch transmitter 2602 according to an embodiment of the invention. Transmitter 2602 comprises four switching devices 2608A, 2608B, 2610A, and 2610B, two aperture generators 2612 and 2614, and two amplifiers 2632 and 2634. Transmitter 2602 is shown having two optional energy storage devices 2613 and 2615.

[0312] The operation of transmitter 2602 is similar to that of transmitter 2402. An information signal to be up-converted is provided to the input(+) port of amplifier 2642. An inverted version of information signal 2642 (i.e., signal 2644) is provided to the input(-) port of amplifier 2634.

[0313] Input signals 2642 and 2644 are operated on by amplifiers 2632 and 2634 in a manner that would be known to a person skilled in the relevant art to produce signals at the outputs of amplifiers 2632 and 2634 that are a function of (i.e., proportional to) the input signals 2642 and 2644. When switches 2608A or 2610B are closed, the output signal of amplifier 2632 is coupled to load impedance 2670, and thereby produces a voltage across load impedance 2670. Similarly, when switches 2608B or 2610A are closed, the output signal of amplifier 2634 is coupled to load impedance 2670, and thereby produces a voltage across load impedance 2670. The operation of switching devices 2608A, 2608B, 2610A and 2610B are controlled by control signals 2646 and 2648, as shown in FIG. 26A. Control signal 2646 controls the switching of switching devices 2408A and 2608B. Control signal 2648 controls the switching of switching devices 2610A and 2610B.

[0314] As described herein, the opening and closing of switching devices 2608A, 2608B, 2610A and 2610B produce a harmonically rich up-converted signal. In embodiments, the up-converted signal is routed to a filter (not shown) to remove the unwanted frequencies that exist as harmonic components of the harmonically rich signal. A desired frequency is optionally amplified by an amplifier module (not shown) and then optionally routed to a transmission module (not shown) for transmission.

[0315] As described herein, optional energy storage devices 2613 and 2615 as well as impedance matching techniques can be used to improve the efficiency of transmitter 2602.

[0316] As seen in FIG. 26A, the architecture of receiver 2602 enhances the amount of energy transferred to the load by using four switches and differential load configurations. Thus, there is about a 3db gain in the output of transmitter 2602 over that of transmitter 2402. A person skilled in the relevant art will understand how transmitter 2502 operates given the description of the invention herein.

[0317] FIGs. 26B-26F are example waveforms that illustrate the operation of transmitter 2602. An information signal 2642 to be up-converted is provided to the input(+) port of amplifier 2632. As shown in FIG. 26B, information signal 2642 is a series of digital bits (1011). An inverted version of information signal 2642 (i.e., signal 2644) is provided to the input(-) port of amplifier 2634. Signal 2644 is shown in FIG. 26C.

[0318] The operation of switching devices 2608A, 2608B, 2610A and 2610B are controlled by control signals 2646 and 2648. These signals are illustrated in FIGs. 26D and 26E. Control signal 2646 controls the switching of switching devices 2608A and 2608B. Control signal 2648 controls the switching of switching devices 2610A and 2610B.

[0319] FIG. 26F illustrates the output signal 2672 of transmitter 2602 for input signals 2642 and 2644. The up-converted signal is obtain from the output signal of transmitter 2602 in a manner similar to that described herein, for example, for a harmonically rich signal.

3.2.3 Enhanced One-Switch Transmitter Embodiments

[0320] As described herein, one-switch transmitter embodiments of the present invention are enhanced to maximize both power transfer and information transmission. These embodiments are described herein for purposes of illustration, and not limitation. Alternate embodiments (including

equivalents, extensions, variations, deviations, etc., of the embodiments described herein), will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments. FIG. 27A is an example one-switch transmitter 2702 according to an embodiment of the invention. Transmitter 2702 comprises one switching device 2708, an aperture generator 2712, two capacitors 2704 and 2706, two impedance devices 2716 and 2718, and two amplifiers 2732 and 2734.

[0321] The operation of transmitter 2702 is similar to that of the other transmitters described above. An input signal 2742 is supplied to amplifier 2732. Input signal 2732 is inverted by an inverter 2703 and the output of inverter 2703 is supplied to the input of amplifier 2734. Amplifiers 2732 and 2734 operate on input signals 2742 and 2744 in a manner that would be known to a person skilled in the relevant arts to produce signals at the outputs of amplifiers 2732 and 2734. When switching device 2708 is open, energy is transferred from the outputs of amplifiers 2732 and 2734 to energy storage devices (capacitors) 2704 and 2706. When switching device 2708 is closed, energy storage devices 2704 and 2706 discharge, thereby transferring energy to load impedance 2770. This causes an output signal 2772 (e.g., as shown in FIG. 27E) to be generated across load impedance 2770. Impedance devices 2716 and 2718 operate as AC chokes (filters).

[0322] FIGs. 27B-27E are example waveforms that illustrate the operation of transmitter 2702. An information signal 2742 to be up-converted shown in FIG. 27B. As shown in FIG. 27B, information signal 2742 is a series of digital bits (1011). An inverted version of information signal 2742 (i.e., signal 2744) is shown in FIG. 27C.

[0323] The operation of switching device 2708 is controlled by control signal 2746. This signal is illustrated in FIG. 27D.

[0324] FIG. 27E illustrates the output signal 2772 of transmitter 2702, which is generated across load impedance 2770. The up-converted signal is obtained

from the output signal of transmitter 2702 in a manner similar to that described elsewhere herein for a harmonically rich signal.

3.2.4 Other Transmitter Embodiments

[0325] The transmitter embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments include, but are not limited to, combinations of modulation techniques in an "I/Q" mode. Such embodiments also include those described in the documents referenced above, such as U.S. Patent Application Ser. Nos. 09/525,615 and 09/550,644. Such alternate embodiments fall within the scope and spirit of the present invention.

[0326] For example, other transmitter embodiments may utilize other modulation techniques. These would be apparent to one skilled in the relevant art(s) based on the teachings disclosed herein, and include, but are not limited to, amplitude modulation (AM), frequency modulation (FM), pulse width modulation, quadrature amplitude modulation (QAM), quadrature phase-shift keying (QPSK), time division multiple access (TDMA), frequency division multiple access (FDMA), code division multiple access (CDMA), embedding two forms of modulation onto a signal for up-conversion, etc., and combinations thereof.

3.3 Transceiver Embodiments

[0327] An exemplary embodiment of a transceiver system 2800 of the present invention is illustrated in FIG. 28. Transceiver 2802 frequency down-converts first EM signal 2808 received by antenna 2806, and outputs down-converted

baseband signal 2812. Transceiver 2802 comprises at least one UFT module 2804 at least for frequency down-conversion.

[0328] Transceiver 2802 inputs baseband signal 2814. Transceiver 2802 frequency up-converts baseband signal 2814. UFT module 2804 provides at least for frequency up-conversion. In alternate embodiments, UFT module 2804 only supports frequency down-conversion, and at least one additional UFT module provides for frequency up-conversion. The up-converted signal is output by transceiver 2802, and transmitted by antenna 2806 as second EM signal 2810.

[0329] First and second EM signals 2808 and 2810 may be of substantially the same frequency, or of different frequencies. First and second EM signals 2808 and 2810 may have been modulated using the same technique, or may have been modulated by different techniques.

[0330] Further example embodiments of receiver/transmitter systems applicable to the present invention may be found in U.S. Patent No. 6,091,940 entitled "Method and System for Frequency Up-Conversion," incorporated by reference in its entirety.

[0331] These example embodiments and other alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the example embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the referenced teachings and the teachings contained herein, and are within the scope and spirit of the present invention. The invention is intended and adapted to include such alternate embodiments.

3.3.1 Example Half-Duplex Mode Transceiver

[0332] An exemplary receiver using universal frequency down conversion techniques is shown in FIG. 29 and described below. An antenna 2902 receives an electromagnetic (EM) signal 2920. EM signal 2920 is routed through a capacitor 2904 to a first terminal of a switch 2910. The other terminal of switch 2910 is connected to ground 2912 in this exemplary

embodiment. A local oscillator 2906 generates an oscillating signal 2928, which is routed through a pulse shaper 2908. The result is a string of pulses 2930. The selection of the oscillator 2906 and the design of the pulse shaper 2908 control the frequency and pulse width of the string of pulses 2930. The string of pulses 2930 control the opening and closing of switch 2910. As a result of the opening and closing of switch 2910, a down converted signal 2922 results. Down converted signal 2922 is routed through an amplifier 2914 and a filter 2916, and a filtered signal 2924 results. In a preferred embodiment, filtered signal 2924 is at baseband, and a decoder 2918 may only be needed to convert digital to analog or to remove encryption before outputting the baseband information signal. This then is a universal frequency down conversion receiver operating in a direct down conversion mode, in that it receives the EM signal 2920 and down converts it to baseband signal 2926 without requiring an IF or a demodulator. In an alternate embodiment, the filtered signal 2924 may be at an "offset" frequency. That is, it is at an intermediate frequency, similar to that described above for the second IF signal in a typical superheterodyne receiver. In this case, the decoder 2918 would be used to demodulate the filtered signal so that it could output a baseband signal 2926.

[0333] An exemplary transmitter using the present invention is shown in FIG. 30. In the FM and PM embodiments, an information signal 3002 modulates an oscillating signal 3006 which is routed to a pulse shaping circuit 3010 which outputs a string of pulses 3011. The string of pulses 3011 controls the opening and closing of the switch 3012. One terminal of switch 3012 is connected to ground 3014, and the second terminal of switch 3012 is connected through a resistor 3030 to a bias/reference signal 3008. In some FM and PM modes, bias/reference signal 3008 is preferably a non-varying signal, often referred to simply as the bias signal. In some AM modes, the oscillating signal 3006 is not modulated, and the bias/reference signal 3008 is a function of the information signal 3004. In one embodiment, information signal 3004 is combined with a bias voltage to generate the reference signal

3008. In an alternate embodiment, the information signal 3004 is used without being combined with a bias voltage. Typically, in the AM mode, this bias/reference signal is referred to as the reference signal to distinguish it from the bias signal used in the FM and PM modes. The output of switch 3012 is a harmonically rich signal 3016 which is routed to an optional "high Q" filter which removes the unwanted frequencies that exist as harmonic components of harmonically rich signal 3016. Desired frequency 3020 is optionally amplified by an optional amplifier module 3022 and routed to transmission module 3024, which outputs a transmission signal 3026. Transmission signal is output by antenna 3028 in this embodiment.

[0334] For the FM and PM modulation modes, FIGs. 31A, 31B, and 31C show the combination of the present invention of the transmitter and the universal frequency down-conversion receiver in the half-duplex mode according to an embodiment of the invention. That is, the transceiver can transmit and receive, but it cannot do both simultaneously. It uses a single antenna 3102, a single oscillator 3144/3154 (depending on whether the transmitter is in the FM or PM modulation mode), a single pulse shaper 3138, and a single switch 3120 to transmit and to receive. In the receive function, "Receiver/transmitter" (R/T) switches 3106, 3108, and 3146/3152 (FM or PM) would all be in the receive position, designated by (R). The antenna 3102 receives an EM signal 3104 and routes it through a capacitor 3107. In the FM modulation mode, oscillating signal 3136 is generated by a voltage controlled oscillator (VCO) 3144. Because the transceiver is performing the receive function, switch 3146 connects the input to the VCO 3144 to ground 3148. Thus, VCO 3144 will operate as if it were a simple oscillator. In the PM modulation mode, oscillating signal 3136 is generated by local oscillator 3154, which is routed through phase modulator 3156. Since the transceiver is performing the receive function, switch 3152 is connected to ground 3148, and there is no modulating input to phase modulator. Thus, local oscillator 3154 and phase modulator 3156 operate as if they were a simple oscillator. One skilled in the relevant art(s) will recognize based on the discussion contained

herein that there are numerous embodiments wherein an oscillating signal 3136 can be generated to control the switch 3120.

[0335] Oscillating signal 3136 is shaped by pulse shaper 3138 to produce a string of pulses 3140. The string of pulses 3140 cause the switch 3120 to open and close. As a result of the switch opening and closing, a down converted signal 3109 is generated. The down converted signal 3109 is optionally amplified and filtered to create a filtered signal 3113. In an embodiment, filtered signal 3113 is at baseband and, as a result of the down conversion, is demodulated. Thus, a decoder 3114 may not be required except to convert digital to analog or to decrypt the filtered signal 3113. In an alternate embodiment, the filtered signal 3113 is at an "offset" frequency, so that the decoder 3114 is needed to demodulate the filtered signal and create a demodulated baseband signal.

[0336] When the transceiver is performing the transmit function, the R/T switches 3106, 3108, and 3146/3152 (FM or PM) are in the (T) position. In the FM modulation mode, an information signal 3150 is connected by switch 3146 to VCO 3144 to create a frequency modulated oscillating signal 3136. In the PM modulation mode switch 3152 connects information signal 3150 to the phase modulator 3156 to create a phase modulated oscillating signal 3136. Oscillation signal 3136 is routed through pulse shaper 3138 to create a string of pulses 3140, which in turn cause switch 3120 to open and close. One terminal of switch 3120 is connected to ground 3142 and the other is connected through switch R/T 3108 and resistor 3123 to a bias signal 3122. The result is a harmonically rich signal 3124 which is routed to an optional "high Q" filter 3126 which removes the unwanted frequencies that exist as harmonic components of harmonically rich signal 3124. Desired frequency 3128 is optionally amplified by amplifier module 3130 and routed to transmission module 3132, which outputs a transmission signal 3134. Again, because the transceiver is performing the transmit function, R/T switch 3106 connects the transmission signal to the antenna 3102.

[0337] In the AM modulation mode, the transceiver operates in the half duplex mode as shown in FIG. 32. The only distinction between this modulation mode and the FM and PM modulation modes described above, is that the oscillating signal 3136 is generated by a local oscillator 3202, and the switch 3120 is connected through the R/T switch 3108 and resistor 3123 to a reference signal 3206. Reference signal 3206 is generated when information signal 3150 and bias signal 3122 are combined by a summing module 3204. It is well known to those skilled in the relevant art(s) that the information signal 3150 may be used as the reference signal 3206 without being combined with the bias signal 3122, and may be connected directly (through resistor 3123 and R/T switch 3108) to the switch 3120.

3.3.2 Example Full-Duplex Mode Transceiver

[0338] The full-duplex mode differs from the half-duplex mode in that the transceiver can transmit and receive simultaneously. Referring to FIG. 33, to achieve this, the transceiver preferably uses a separate circuit for each function. A duplexer 3304 is used in the transceiver to permit the sharing of an antenna 3302 for both the transmit and receive functions.

[0339] The receiver function performs as follows. The antenna 3302 receives an EM signal 3306 and routes it through a capacitor 3307 to one terminal of a switch 3326. The other terminal of switch 3326 is connected to ground 3328, and the switch is driven as a result of a string of pulses 3324 created by local oscillator 3320 and pulse shaper 3322. The opening and closing of switch 3326 generates a down converted signal 3314. Down converted signal 3314 is routed through a amplifier 3308 and a filter 3310 to generate filtered signal 3316. Filtered signal 3316 may be at baseband and be demodulated or it may be at an "offset" frequency. If filtered signal 3316 is at an offset frequency, decoder 3312 will demodulate it to create the demodulated baseband signal 3318. In a preferred embodiment, however, the filtered signal 3316 will be a demodulated baseband signal, and decoder 3312 may not be required except to

convert digital to analog or to decrypt filtered signal 3316. This receiver portion of the transceiver can operate independently from the transmitter portion of the transceiver.

[0340] The transmitter function is performed as follows. In the FM and PM modulation modes, an information signal 3348 modulates an oscillating signal 3330. In the AM modulation mode, the oscillating signal 3330 is not modulated. The oscillating signal is shaped by pulse shaper 3332 and a string of pulses 3334 is created. This string of pulses 3334 causes a switch 3336 to open and close. One terminal of switch 3336 is connected to ground 3338, and the other terminal is connected through a resistor 3347 to a bias/reference signal 3346. In the FM and PM modulation modes, bias/reference signal 3346 is referred to as a bias signal 3346, and it is substantially non-varying. In the AM modulation mode, an information signal 3350 may be combined with the bias signal to create what is referred to as the reference signal 3346. The reference signal 3346 is a function of the information signal 3350. It is well known to those skilled in the relevant art(s) that the information signal 3350 may be used as the bias/reference signal 3346 directly without being summed with a bias signal. A harmonically rich signal 3352 is generated and is filtered by a "high Q" filter 3340, thereby producing a desired signal 3354. The desired signal 3354 is amplified by amplifier 3342 and routed to transmission module 3344. The output of transmission module 3344 is transmission signal 3356. Transmission signal 3356 is routed to duplexer 3304 and then transmitted by antenna 3302. This transmitter portion of the transceiver can operate independently from the receiver portion of the transceiver.

[0341] Thus, as described above, the transceiver embodiment the present invention as shown in FIG. 33 can perform full-duplex communications in all modulation modes.

3.3.3 Enhanced Single Switch Transceiver Embodiment

[0342] As described herein, one-switch transceiver embodiments of the present invention are enhanced to maximize power transfer and information extraction and transmission. These embodiments are described herein for purposes of illustration, and not limitation. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0343] FIG. 34 is an example one-switch transceiver 3402 according to an embodiment of the invention The operation of this embodiment as a receiver is described above with regard to FIGs. 18A-E. The operation of this embodiment as a transmitter is described above with regard to FIGs. 27A-E. Also described above is a means for coupling receiver and transmitter embodiments of the invention to an antenna. Thus, given the description herein, a person skilled in the relevant arts will understand the operation of transceiver 3402.

3.3.4 Other Embodiments

[0344] The embodiments described above are provided for purposes of illustration. These embodiments are not intended to limit the invention. Alternate embodiments, differing slightly or substantially from those described herein, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Such alternate embodiments fall within the scope and spirit of the present invention.

4 Enhanced Operating Features of the Invention

[0345] As described herein, embodiments of the present invention have enhanced operating features. These enhanced features enable receivers and transceivers according to the invention to down-convert a modulated carrier signal while extracting power from the carrier signal. This is in contrast to conventional receivers and transceivers, which ideally extract zero power from a received carrier signal (i.e., conventional receivers are typically designed to operate as impulse samplers). These enhanced features of the present invention also enable the linear operating ranges for embodiments of the invention to be extended.

4.1 Enhanced Power and Information Extraction Features

[0346] Enhanced features of the invention enable the invention to down-convert a modulated carrier signal while extracting power from the signal. These features are not found in conventional receivers.

[0347] As described herein, embodiments of the invention are implemented using one or more aliasing modules 300 (see for example FIGs. 3A and 3G). Differences between receiver embodiments according to the present invention and conventional receivers are illustrated in FIG. 36-41. For example, consider aliasing module 300 as shown in FIG. 3A. Aliasing module 300 down-converts an input signal 304 to form an output signal 312 as described herein.

[0348] FIG. 36 illustrates a modulated carrier signal 3602 that can be down converted using either an aliasing module 300 or a conventional receiver. Signal 3602 has a period of T_C.

[0349] In this example, to down convert signal 3602 using a conventional receiver, signal 3602 is sampled using a control signal 3702 illustrated in FIG. 37. Control signal 3702 comprises a plurality of sampling impulses 3704. Each impulse 3704 ideally has a zero-width aperture. The sampling period of

control signal 3700 must satisfy Nyquests' sampling criteria (i.e., it must be equal to or less than one-half T_C).

[0350] In contrast to a conventional receiver, to down convert signal 3602 according to the invention, a control signal, for example control signal 3802 shown in FIG. 38, is used. As can be seen in FIG. 38, control signal 3802 comprises sampling apertures having significant width compared to zero-width sampling impulses 3704 of control signal 3702. The width of the sampling apertures of control signal 3802 are T_A.

[0351] Control signal 3802 is shown having both positive magnitude apertures and negative magnitude apertures. In embodiments of the invention having two aliasing modules 300, the positive magnitude apertures control one aliasing module 300, and the negative magnitude apertures control another aliasing module 300, as described above. For embodiments of the invention having only one aliasing module 300, a control signal having only the positive magnitude apertures or the negative magnitude apertures of control signal 3802 can be used, as described herein. The period of time between two adjacent positive magnitude apertures or two adjacent negative magnitude apertures is T_D. As shown in FIG. 38, T_D is greater than T_C.

4.2 Charge Transfer and Correlation

[0352] The description of the invention that follows teaches one skilled in the relevant arts how to determine a value for one or more capacitors to be used in embodiments of the invention. As described herein, a significant difference between conventional communications systems and the present invention is that conventional communications systems are not intended to transfer non-negligible amounts of energy from a carrier signal to be used in forming a down-converted information signal (i.e., conventional communications system do not exhibit the capacitor discharge feature of the present invention). As illustrated in FIG. 39, the voltage signal across a capacitor, for example, of a conventional sample and hold communications system ideally remains

constant (i.e., there is no energy transfer or intended discharge of the charge stored by the capacitor.) In contrast, as illustrated in FIG. 40, and as described herein with regards to embodiments of the invention, energy transfer is a feature of the present invention and capacitors (such as capacitor 310 in FIG. 3A and capacitor 310 in FIG. 3G) used in embodiments of the invention are sized to achieve a percent discharge between apertures of a switching (control) signal.

[0353] In embodiments of the invention such as, for example, aliasing modules 300, one or more capacitors are sized to discharge between about six percent to about fifty percent of the total charge stored therein during a period of time that a switching device is open (i.e., between apertures). It is noted that this range is provided for illustrative purposes. Other embodiments of the invention exhibit other discharge percentages. FIG. 41 illustrates the voltage across a capacitor sized according to the invention for different rates of discharge (i.e., charge transfer).

[0354] The basic equation for charge transfer is:

$$\frac{dq}{dt} = C\frac{dv}{dt}, \text{ (assuming C is constant over time)} \qquad \text{EQ. (2)}$$

$$q = CV$$

[0355] Similarly the energy u stored by a capacitor can be found from:

$$u = \int_0^q \frac{q_x}{C}\, dq_x = \frac{q^2}{2C} \qquad \text{EQ. (3)}$$

[0356] From EQs. (2) and (3):

$$u = \frac{Cv^2}{2} \qquad \text{EQ. (4)}$$

[0357] Thus, the charge stored by a capacitor is proportional to the voltage across the capacitor, and the energy stored by the capacitor is proportional to the square of the charge or the voltage. Hence, by transferring charge, voltage and energy are also transferred. If little charge is transferred, little energy is transferred, and a proportionally small voltage results unless C is lowered.

[0358] The law of conversation of charge is an extension of the law of the conservation of energy. EQ. (2) illustrates that if a finite amount of charge must be transferred in an infinitesimally short amount of time then the voltage, and hence voltage squared, tends toward infinity. Furthermore,

$$V_c = \frac{1}{C}\int_0^{T_A} idt \qquad \text{EQ. (5)}$$

[0359] This implies an infinite amount of current must be supplied to create the infinite voltage, if T_A is infinitesimally small. As will be understood by a person skilled in the relevant art, such a situation is impractical, especially for a device without gain.

[0360] Generally speaking, in radio communications systems, the antenna produces a small amount of power available for the first conversion, even with amplification from an LNA. Hence, if a finite voltage and current restriction do apply to the front end of a radio then a conversion device, which is an impulse sampler, must by definition possess infinite gain. This would not be practical for a switch. What is usually approximated in practice is a fast sample time, charging a small capacitor, then holding the value acquired by a hold amplifier, which preserves the voltage from sample to sample (i.e., a sample and hold system is used).

[0361] The analysis that follows shows that given a finite amount of time for energy transfer through a conversion device, the impulse response of the ideal processor, which transfers energy to a capacitor when the input voltage source is a sinusoidal carrier and possesses a finite source impedance, is achieved by embodiments of the present invention. If a significant amount of energy can be transferred in the sampling process, the tolerance on the charging capacitor can be reduced and the requirement for a hold amplifier is significantly reduced or even eliminated.

[0362] In embodiments, the maximum amount of energy available over a half sine pulse can be found from:

$$u = \int_0^{T_A} S_i^2(t)dt = \frac{A^2 T_A}{2} \qquad (A^2\pi/2 \text{ for } \omega_c = 1) \qquad \text{EQ. (6)}$$

[0363] This points to a correlation processor or matched filter processor. If energy is of interest then a useful processor, which transfers all of the half sine energy, is revealed in EQ. (5), where T_A is an aperture equivalent to the half sine pulse. In embodiments, EQ. (6) provides the insight to an enhanced processor.

[0364] Consider the following equation sequence:

$$\int_0^{\infty} h(\tau)S_i(t-\tau)d\tau \Rightarrow \int_0^{T_A} kS_i^2(T_A-\tau)d\tau \Rightarrow \int_{-0}^{T_A} S_i^2(t)dt \qquad \text{EQ. (7)}$$

where $h(\tau) = S_i(T_A - \tau)$ and $t = T_A - \tau$. This is a matched filter equation with the far most right hand side revealing a correlator implementation, which is obtained by a change of variables as indicated. Note that the correlator form of the matched filter is a statement of the desired signal energy. Therefore a matched filter/correlator accomplishes acquisition of all the energy available across a finite duration aperture. Such a matched filter/correlator can be implemented as shown in FIG. 54.

[0365] In embodiments, when configured for enhanced operation, the example matched filter/correlator of FIG. 54 operates in synchronism with the half sine pulse $S_i(t)$ over the aperture T_A. Phase skewing and phase roll will occur for clock frequencies, which are imprecise. Such imprecision can be compensated for by a carrier recovery loop, such as a Costas Loop. A Costas Loop can develop the control for the acquisition clock, which also serves as a sub-harmonic carrier. However, phase skew and non-coherency does not invalidate the enhanced form of the processor provided that the frequency or phase errors are small, relative to T^{-1}_A. Non-coherent and differentially coherent processors may extract energy from both I and Q with a complex correlation operation followed by a rectifier or phase calculator. It has been shown that phase skew does not alter the optimum SNR processor formulation. The energy that is not transferred to I is transferred to Q and vice versa when phase skew exists. This is an example processor for a finite duration sample window with finite gain sampling function, where energy or charge is the desired output.

[0366] Some matched filter/correlator embodiments according to the present invention might, however, be too expensive and complicated to build for some applications. In such cases, other processes and processors according to embodiments of the invention can be used. The approximation to the matched filter/correlator embodiment shown in FIG. 55 is one embodiment that can be used in such instances. The finite time integrator embodiment of FIG. 55 requires only a switch and an integrator. This embodiment of the present invention has only a 0.91dB difference in SNR compared to the matched filter/correlator embodiment.

[0367] Another low cost and easy to build embodiment of the present invention is an RC processor. This embodiment, shown in FIG. 56, utilizes a low cost integrator or capacitor as a memory across the aperture. If C is suitably chosen for this embodiment, its performance approaches that of the matched filter/correlator embodiment, shown in FIG. 54. Notice the inclusion of the source impedance, R, along with the switch and capacitor. This embodiment nevertheless can approximate the energy transfer of the matched filter/correlator embodiment.

[0368] When maximum charge is transferred, the voltage across the capacitor 5604 in FIG. 56 is maximized over the aperture period for a specific RC combination.

[0369] Using EQs. (2) and (5) yields:

$$q = C \cdot \frac{1}{C} \int_0^{T_A} i_c dt \qquad \text{EQ. (8)}$$

[0370] If it is accepted that an infinite amplitude impulse with zero time duration is not available or practical, due to physical parameters of capacitors like ESR, inductance and breakdown voltages, as well as currents, then EQ. (8) reveals the following important considerations for embodiments of the invention:

The transferred charge, q, is influenced by the amount of time available for transferring the charge;

The transferred charge, q, is proportional to the current available for charging the energy storage device; and

Maximization of charge, q, is a function of i_c, C, and T_A.

[0371] Therefore, it can be shown that for embodiments:

$$q_{max} = Cv_{max} = C\left[\frac{1}{C}\int_0^{T_A} i_c dt\right]_{max} \qquad \text{EQ. (9)}$$

[0372] The impulse response for the RC processing network is;

$$h(t) = \frac{e^{\frac{-\tau}{RC}}}{RC}[u(\tau) - u(\tau - T_A)] \qquad \text{EQ. (10)}$$

[0373] Suppose that T_A is constrained to be less than or equal to $^1/_2$ cycle of the carrier period. Then, for a synchronous forcing function, the voltage across a capacitor is given by EQ. (11).

$$V_0(t) = \int_{-\infty}^{t} \sin(\pi f_A \tau) \cdot \frac{e^{\frac{-(t-\tau)}{RC}}}{RC} d\tau \qquad \text{EQ. (11)}$$

[0374] Maximizing the charge, q, requires maximizing V_0 (t) with respect to t and β.

$$\frac{\partial^2 V_0(t)}{\partial t \, \partial \beta} = \dot{0} \qquad \text{EQ. (12)}$$

[0375] It is easier, however, to set R = 1, T_A = 1, A =1, $f_A = T_A^{-1}$ and then calculate $q = cV_0$ from the previous equations by recognizing that $q = \frac{\beta^{-1}}{R} V_0 = cV_0$, which produces a normalized response.

[0376] FIG. 57 illustrates that increasing C is preferred in various embodiments of the invention. It can be seen in FIG. 57 that as C increases (i.e., as β decreases) the charge transfer also increases. This is what is to be expected based on the optimum SNR solution. Hence, for embodiments of the present invention, an optimal SNR design results in optimal charge transfer. As C is increased, bandwidth considerations should be taken into account.

[0377] In embodiments, EQ. (6) establishes T_A as the entire half sine for an optimal processor. However, in embodiments, optimizing jointly for t and β

reveals that the RC processor response creates an output across the energy storage capacitor that peaks for $t_{max} \cong .75T_A$, and $\beta_{max} \cong 2.6$, when the forcing function to the network is a half sine pulse.

[0378] In embodiments, if the capacitor of the RC processor embodiment is replaced by an ideal integrator then $t_{max} \rightarrow T_A$.

$$\beta T_A \simeq 1.95 \qquad \text{EQ. (13)}$$

where $\beta = (RC)^{-1}$

[0379] For example, for a 2.45 GHz signal and a source impedance of 50Ω, EQ. (13) above suggests the use of a capacitor of ≅ 2pf. This is the value of capacitor for the aperture selected, which permits the optimum voltage peak for a single pulse accumulation. For practical realization of some embodiments of the present invention, the capacitance calculated by EQ. (13) is a minimum capacitance. SNR is not considered optimized at $\beta T_A \simeq 1.95$. A smaller β yields better SNR and better charge transfer. In embodiments, it turns out that charge can also be enhanced if multiple apertures are used for collecting the charge.

[0380] In embodiments, for the ideal matched filter/correlator approximation, βT_A is constant and equivalent for both consideration of enhanced SNR and enhanced charge transfer, and charge is accumulated over many apertures for most practical designs. Consider the following example, $\beta = .25$, and $T_A = 1$. Thus $\beta T_A = .25$. At 2.45 GHz, with R =50Ω, C can be calculated from:

$$C \geq \frac{T_A}{R(.25)} \geq 16.3pf \qquad \text{EQ. (14)}$$

[0381] The charge accumulates over several apertures, and SNR is simultaneously enhanced melding the best of two features of the present invention. Checking CV for $\beta T_A \simeq 1.95$ vs. $\beta T_A = .25$ confirms that charge is enhanced for the latter.

4.3 Load Resistor Consideration

[0382] FIG. 58 illustrates an example RC processor embodiment 5802 of the present invention having a load resistance 5804 across a capacitance 5806. As will be apparent to a person skilled in the relevant arts given the description of the invention herein, RC processor 5802 is similar to an aliasing module and/or an energy transfer module according to the invention.

[0383] The transfer function of An RC processing embodiment 5802 of the invention (without initial conditions) can be represented by the following equations:.

$$H(s)=\frac{1-e^{-sT_A}}{s}\left(\frac{1}{sCR+k}\right) \qquad \text{EQ. (15)}$$

$$k=\left(R/R_L+1\right) \qquad \text{EQ. (16)}$$

$$h(t)=\left(\frac{e^{-\frac{t\cdot k}{RC}}}{RC}\right)\left[u(t)-(t-T_A)\right] \qquad \text{EQ. (17)}$$

[0384] From the equations, it can be seen that R_L 5804, and therefore k, accelerate the exponential decay cycle.

$$V_0(t)=\int_{-\infty}^{t}\sin(\pi f_a\tau)\cdot\frac{e^{-\frac{k(t-\tau)}{RC}}}{RC}\,d\tau \qquad \text{EQ. (18)}$$

$$V_0(t)=\left(\frac{1}{k^2+(\pi f_A)^2}\right)\left[k\cdot\sin(\pi f_A t)-\pi f_A RC\cdot\cos(\pi f_A t)+RCe^{-\frac{kt}{RC}}\right]\quad 0\le t\le T_A$$

EQ.(19)

[0385] This result is valid over the acquisition aperture. After the switch is opened, the final voltage that occurred at the sampling instance $t \cong T_A$ becomes an initial condition for a discharge cycle across R_L 5804. The discharge cycle possesses the following response:

$$V_D=\frac{V_A\cdot e^{-\frac{t}{R_LC}}}{R_LC}u(t-T_A)\ \textit{(single event discharge)} \qquad \text{EQ. (20)}$$

[0386] V_A is defined as $V_0(t \cong T_A)$. Of course, if the capacitor 5806 does not completely discharge, there is an initial condition present for the next acquisition cycle.

[0387] FIG. 59 illustrates an example implementation of the invention, modeled as a switch S, a capacitor C_S, and a load resistance R. FIG. 61 illustrates example energy transfer pulses, having apertures A, for controlling the switch S. FIG. 60 illustrates an example charge/discharge timing diagram for the capacitor C_S, where the capacitor C_S charges during the apertures A, and discharges between the apertures A.

[0388] Equations (21) through (35) derive a relationship between the capacitance of the capacitor C_S ($C_S(R)$), the resistance of the resistor R, the duration of the aperture A (aperture width), and the frequency of the energy transfer pulses (freq LO) in embodiments of the invention. EQ. (31) illustrates that in an embodiment optimum energy transfer occurs when x = 0.841 (i.e., in this example, the voltage on the capacitor at the start of the next aperture (charging period) is about 84.1 percent of the voltage on the capacitor at the end of the preceding aperture (charging period)). Based on the disclosure herein, one skilled in the relevant art(s) will realize that values other that 0.841 can be utilized (See, for example, FIG. 41).

$$\phi = \frac{1}{C}\int i(t)\partial t + Ri(t) \qquad \text{EQ. (21)}$$

$$\frac{\partial}{\partial t}\phi = \frac{\partial}{\partial t}\left[\frac{1}{C}\int i(t)\partial t + Ri(t)\right] \qquad \text{EQ. (22)}$$

$$\phi = \frac{i(t)}{C_s} + \frac{R\partial i(t)}{\partial t} \qquad \text{EQ. (23)}$$

$$\phi = \frac{1}{C_s} + R \cdot s \qquad \text{EQ. (24)}$$

$$s = \frac{-1}{C_s \cdot R}, \text{ by definition: } i_{init}(t) = \frac{V_{C_s}\,init}{R} \qquad \text{EQ. (25)}$$

$$i(t) = \left(\frac{V_{C_s}\,init}{R}\right) \cdot e^{\left(\frac{-t}{C_s \cdot R}\right)} \qquad \text{EQ. (26)}$$

$$V_{out}(t) = R \cdot i(t) = V_{C_s} init \cdot e\left(\frac{-t}{C_s \cdot R}\right) \quad \text{EQ. (27)}$$

[0389] Maximum power transfer occurs when:

$$Power\_Final = \frac{1}{\sqrt{2}} \cdot Peak\_Power \quad \text{EQ. (28)}$$

$$Power\_Peak = \frac{\left(V_{C_s} peak\right)^2}{R} \quad \text{EQ. (29)}$$

$$Power\_Final = \frac{\left(x \cdot V_{C_s} peak\right)^2}{R} \quad \text{EQ. (30)}$$

[0390] Using substitution:

$$\frac{\left(x \cdot V_{C_s} peak\right)^2}{R} = \frac{\left(V_{C_s} peak\right)^2}{R} \cdot \frac{1}{\sqrt{2}} \quad \text{EQ. (31)}$$

[0391] Solving for "x" yields: x = 0.841.

[0392] Letting $V_{Cs}init = 1$ yields $V_{out}(t) = 0.841$ when

$$t = \frac{1}{freqLO} - Aperture\_Width. \quad \text{EQ. (32)}$$

[0393] Using substitution again yields:

$$0.841 = 1 \cdot e^{\left(\frac{\frac{1}{freqLO} - Aperture\_Width}{-C_s \cdot R}\right)} \quad \text{EQ. (33)}$$

$$\ln(0.841) = \left(\frac{\frac{1}{freqLO} - Aperture\_Width}{-C_s \cdot R}\right) \quad \text{EQ. (34)}$$

[0394] This leads to the following EQ. (35) for selecting a capacitance.

$$C_s(R) = \left(\frac{\frac{1}{freqLO} - Aperture\_Width}{-\ln(0.841) \cdot R}\right) \quad \text{EQ. (35)}$$

[0395] The following equation according to the invention can be solved to find an expression for the energy accumulated over a bit time, Eb, as shown below.

$$D = \int_0^{T_A} \left(u(t) - u\left(t - T_A\right)\right) \cdot A\sin\left(2\pi ft + \theta\right)dt \qquad \text{EQ. (36)}$$

$$D = A\cos(\theta) \cdot \frac{\left(-\cos\left(2\pi ft\right)\right)}{(2\pi)f} \quad \text{(Evaluated from 0 to } T_A\text{)} \qquad \text{EQ. (37)}$$

where u(t), u(t-T_A), and A are in volts, and D is expressed in Volts*Volts/Hz.

[0396] Realizing the f equals 1/t, D can be written as:

$$D = A\cos(\theta) \cdot \frac{\left(-\cos\left(2\pi ft\right)t\right)}{(2\pi)} \qquad \text{EQ. (38)}$$

where D is now expressed in volts*volts*seconds.

[0397] Dividing D by the complex impedance Z of an RC processor according to the invention, when the switch (aperture) is closed, results in:

$$\frac{D}{Z} = A\cos(\theta) \cdot \frac{\left(-\cos\left(2\pi ft\right)t\right)}{(2\pi)Z} \quad \text{(Evaluated from 0 to } T_A\text{)} \qquad \text{EQ. (39)}$$

Since (volts*volts)/Z equals power, and since power equals joules/second, D/Z has units of (joules/second)/second. Thus, D/Z is the amount of energy accumulated over a bit time (Eb).

[0398] A more useful expression for the energy accumulated over a bit time (Eb) is:

$$E_b = \sum_{n=1}^{aperturep\_per\_bit} A_n \cos\left(\theta_n\right)\left(\frac{-\cos\left(2\pi ft\right)t}{2\pi Z_n}\right) \text{(Evaluated from 0 to } T_A\text{)} \qquad \text{EQ. (40)}$$

where Eb is expressed in joules per bit.

[0399] Referring to the following equation, from above, it can be seen that there is a $2\pi f$ term in the denominator.

$$D = A \cdot \cos\left(\phi\right) \cdot \frac{\left(-\cos\left(2 \cdot \pi \cdot f \cdot t\right)\right)}{(2 \cdot \pi) \cdot f} \qquad \text{EQ. (41)}$$

Analysis reveals that this term, and other terms, have physical units that allow a person skilled in the relevant art, given the discussion herein, to understand and relate the resultant quantity in a manner consistent with actual measurements of implementations of the present invention.

[0400] Note that as the aperture time Ta becomes smaller, the absolute value of the energy accumulated over a single aperture period is less. However, what is equally important is the fact that the energy continues to accumulate over multiple aperture periods. The number of aperture periods required to reach an optimum value is dependent on two factors: (1) the aperture period, and (2) the complex impedance (Z) of C and R when the switch is closed, as described elsewhere herein. The values of C and R can, therefore, be selected to optimize the energy transfer during the half sine sample period. By including the Z term in the equation, a person skilled in the relevant art can calculate the Energy per Bit (i.e., Eb) directly and relate the results back to embodiments of the present invention, e.g., hardware performance. This analysis can also be used to show that the optimum system performance in terms of bandwidth and power transfer occurs when the aperture period is equal to one-half of a carrier frequency cycle.

4.4 Enhancing the Linear Operating Features of Embodiments of the Invention

[0401] The analysis and description that follow explain how to enhance the linearity of embodiments of the invention. As described herein, embodiments of the present invention provide exceptional linearity per milliwatt. For example, rail to rail dynamic range is possible with minimal increase in power. In an example integrated circuit embodiment, the present invention provides +55dmb IP2, +15 dbm IP3, @ 3.3V, 4.4ma, -15dmb LO. GSM system requirements are +22dbm IP2, -10.5dmb IP3. CDMA system requirements are +50dmb IP2, +10dbm IP3.

[0402] As described herein, embodiments of the invention can be implemented using MOSFETs (although the invention is not limited to this example). Thus, for purposes of analysis, it is assumed that an embodiment of the invention is implemented using one or more enhancement MOSFETs having the following parameter:

a channel width (W) equal to 400 microns;

a channel length (L) of 0.5 microns;

a threshold voltage (Vt) equal to 2 volts; and

a k value equal to 0.003 (W/L), or k equal to 0.24.

[0403] The drain current (I_D) for an N-Channel Enhancement MOSFET is given by the following 2nd order equation:

$$i_D(v_{GS}, v_{DS}) := \begin{cases} K\cdot\left[2\cdot(v_{GS}-V_t)\cdot v_{DS}-v_{DS}^2\right] & \text{if } v_{DS}\le v_{GS}-V_t \\ \left[K\cdot(v_{GS}-V_t)^2\right] & \text{otherwise} \end{cases} \qquad \text{EQ. (42)}$$

[0404] Note that since EQ. 42 is only a second order equation, we analyze second order distortion.

[0405] FIG. 42 is a plot of drain current (I_D) as a function of drain-source voltage (V_{DS}) for three different gate-source voltages (i.e., Vgs equal to 3V, 4V, and 5V). As evident from the i_D versus v_{DS} plot in FIG. 42, the larger the gate-source voltage $_{is,}$ the larger the linear region (larger "ohmic" or "triode" region) is for v_{DS}. The linear region is represented by the sloped lines (linear resistances) just to the left of the knee of the curves. The drain current distorts when v_{DS} starts swinging beyond the sloped line, into the knee of the curve.

[0406] FIG. 43 is a plot of the drain current of a typical FET as a function of drain-source voltage and gate-source voltage. It illustrates how linearity is improved by increasing the gate-source voltage. Of particular note, FIG. 43 shows that a FET becomes increasingly linear with increasing v_{GS}.

[0407] FIG. 43 shows how the drain current of a FET distorts when a sinusoid $V_{DS}(t)$ is applied across the drain and source junction. Therefore, biasing the FET with a larger V_{GS} improves linearity.

[0408] FIG. 44 illustrates what happens when, instead of having a large constant V_{GS}, V_{GS} is made to change proportionally to V_{DS}. In FIG. 44, three different constants of proportionality have been plotted to illustrate what

happens to the linearity when V_{GS} is made to change proportionally to V_{DS}. Each of the curves is plotted with the same DC bias of 3 volts on V_{GS}. The first curve has a constant of proportionality of zero (i.e., no change of V_{GS} with V_{DS}).

[0409] As illustrated by the curves in FIG. 44, in embodiments, one can get an additional, significant linearity improvement over the large and constant V_{GS} case, if one makes V_{GS} change proportionally to V_{DS}. Furthermore, as shown in FIG. 44, there is an optimum constant of proportionality (i.e., 0.5) in embodiments of the invention.

[0410] FIGs. 45A-E are plots of the FFTs of the FET drain currents for different constants of proportionality (CPs). These plots illustrate how second order distortion is affected when using different constants of proportionality. The second order distortion in FIG. 45A (PC=0) is –12.041 dBc. The second order distortion in FIG. 45B (PC=0.25) is –18.062 dBc. The second order distortion in FIG. 45C (PC=0.5) is –318.443 dBc. The second order distortion in FIG. 45D (PC=0.75) is –18.062 dBc. The second order distortion in FIG. 45E (PC=1) is –12.041 dBc.

[0411] The plots in FIGs. 45A-E show that there is a significant linearity improvement by making V_{GS} change proportional to V_{DS} over the case where V_{GS} is constant. The optimum constant of proportionality is 0.5, or when V_{GS} is proportional to V_{DS} by a factor of 0.5. It can be shown that choosing constants of proportionality greater than 1 will make the FET linearity worse than having a constant V_{GS} (PC = 0). FIGs. 45A-E show, as expected, that the DC term increases as the second order distortion gets worse (i.e., second order distortion produces a DC term).

[0412] FIG. 46 shows two sets of curves. One set of curves is a plot of the FET drain current with a constant V_{GS}. The other set of curves is a plot of the FET drain current with a V_{GS} signal proportional to one half V_{DS}. The FET linearization effect can be seen in FIG. 46.

[0413] The FET linearization effect can also be seen mathematically by substituting $V_{GS} = V_{bias} + 0.5V_{DS}$ into the FET's drain current equation above to obtain:

$$i_D(v_{DS}) = \begin{cases} K\cdot\left[2\cdot\left[\left(V_{bias} + 0.5\cdot v_{DS}\right) - V_t\right]\cdot v_{DS} - v_{DS}^2\right] & \text{if } v_{DS} \le V_{bias} + 0.5\cdot v_{DS} - V_t \\ \left[K\cdot\left(V_{bias} + 0.5\cdot v_{DS} - V_t\right)^2\right] & \text{otherwise} \end{cases}$$

EQ. (43)

[0414] Simplifying this expression yields:

$$i_D(v_{DS}) := \begin{cases} \left[2\cdot K\cdot\left(V_{bias} - V_t\right)\right]\cdot v_{DS} & \text{if } v_{DS} \le 2\cdot\left(V_{bias} - V_t\right) \\ 0.25\cdot K\cdot\left[v_{DS} + 2\cdot\left(V_{bias} - V_t\right)\right]^2 & \text{otherwise} \end{cases}$$

EQ. (44)

[0415] Thus, for v_{DS} less than or equal to $2(V_{bias} - V_t)$, the drain current is a linear function of v_{DS} with a slope of $2K(V_{bias} - V_t)$. In this region, making V_{GS} equal to half of V_{DS}, cancels the square term $(V_{DS})^2$, leaving only linear terms.

[0416] As described herein, embodiments of the invention (see, for example, the embodiments illustrated in FIGs. 18A and 19) exhibit enhanced linearity properties. The enhanced linearity properties are achieved where:

(1) $|V_{GS}| \geq 0.5 * Vdd$ (i.e., the instantaneous differential voltage $|V_{GS}|$ is made as large as possible for both NMOS and PMOS devices, thus ensuring that voltage differential $|V_{GS}|$ does not swing below (0.5 * Vdd)),

(2) $|V_{GS}| = |0.5 * V_{DS}| + 0.5 * Vdd$ (i.e., as the RF signal across the drain and source gets larger, the voltage differential $|V_{GS}|$ gets larger by a proportionality factor of 0.5 -- when the RF signal gets large and one needs more linearity, V_{GS} automatically increases to give more linearity), and/or

(3) The drain and source of the NMOS and PMOS devices swap every half RF cycle so that (1) and (2) above are always satisfied.

[0417] If an amplitude imbalance occurs, for example, across the FETS in FIG. 19, it will degrade the 2nd order linearity performance of receiver 1902. This is because the amplitude imbalance will change the constant of

proportionality relating v_{GS} to v_{DS} from the optimum value of 0.5 to some other value. However, the only amplitude imbalance possible is at RF because the configuration of receiver 1902 guarantees that the baseband waveform will have perfect phase and amplitude balance.

[0418] In addition to the advantages already described herein, additional advantages of receiver 1902 include: lower LO to RF reradiation, lower DC offset, and lower current (only one switch). Furthermore, the architecture of receiver 1902 ensures that the baseband differential signals will be amplitude and phase balanced, regardless of the imbalance at the input of the circuit at RF. This is because when the FET switch turns on, the two input capacitors are shorted together in series with a differential voltage across them. The capacitors have no ground reference and thus do not know there is an imbalance. As will be apparent to a person skilled in the relevant arts, the advantages to the configuration of receiver 1902 and UFD module 1938 are significant. In practice, the differential configuration of UFD 1938 has yielded high linearity that is repeatable.

[0419] In summary, to enhance the linearity of embodiments of the invention, one should:

(1) maintain the instantaneous voltage differential V_{GS} as large as possible for both the NMOS and PMOS devices; and/or

(2) make the voltage differential V_{GS} change proportional to V_{DS} so that $|V_{GS}| = V_{bias} + 0.5 * |V_{DS}|$.

[0420] The enhanced linearity features described herein are also applicable to single-switch embodiments of the invention. Consider, for example, the embodiment shown in FIG. 20E. For this embodiment, V_{GS} increases with V_{DS} over half of an RF cycle. During the other half of the cycle V_{GS} is constant. During the half RF cycle that V_{GS} does increase with V_{DS}, it increases at the same rate as V_{DS}. The magnitude of V_{GS} is given by EQ. 45 and EQ. 46.

$$| V_{GS} | = | V_{DS} | + 0.5 * Vdd \quad \text{(for negative half of RF cycle)} \qquad \text{EQ. (45)}$$

$|V_{GS}| = 0.5 * Vdd$ (for positive half of RF cycle) EQ. (46)

[0421] FIGs. 47-53 further illustrate the enhanced linearity features of embodiments of the invention.

[0422] FIG. 47 shows additional plots that illustrate how the linearity of switching devices are enhance, for example, by the architecture of FIG. 19. FIG. 19 shows the current of the switching device when used according to the architecture of a conventional receiver and the architecture of receiver 1902. As described herein, the current of a typical FET switching device is given by EQ. 47 below, and the current of the FET switching device when used according to the embodiment shown in FIG. 19 is given by EQ. 48.

$$id(vgs, vds) := \begin{cases} K\cdot\left[2\cdot(vgs - vt)\cdot vds - vds^2\right] & \text{if } vds \le vgs - vt \\ \left[K\cdot(vgs - vt)^2\right] & \text{otherwise} \end{cases} \quad \text{EQ. (47)}$$

$$id1(vgs, vds) := \begin{cases} K\cdot\left[2\cdot(vgs + c\cdot vds - vt)\cdot vds - vds^2\right] & \text{if } vds \le (vgs + c\cdot vds - vt) \\ \left[K\cdot(vgs + c\cdot vds - vt)^2\right] & \text{otherwise} \end{cases} \quad \text{EQ. (48)}$$

where k = 0.24, vt = 1.2 volts, c = 0.5, and Vds = 0 to 5 volts.

[0423] FIG. 47 illustrates the current of a typical FET switching device when used in a conventional receiver (id), when used in receiver 1902 (id1), and when used in receiver 2002 (id2). EQ. 49 describes the current in a typical FET switching device. EQ. 50 describes the current in a FET of receiver 1902. EQ. 51 describes the current in a FET of receiver 2002.

$$id(vgs, vds, t) := \begin{cases} K\cdot\left[2\cdot(vgs - vt)\cdot vds(t) - vds(t)^2\right] & \text{if } vds(t) \le vgs - vt \\ \left[K\cdot(vgs - vt)^2\right] & \text{otherwise} \end{cases} \quad \text{EQ. (49)}$$

$$id2(vgs, vds, t) := \begin{cases} K\cdot\left[2\cdot(vgs + c\cdot vds(t) - vt)\cdot vds(t) - vds(t)^2\right] & \text{if } vds(t) \le (vgs + c\cdot vds(t) - vt) \\ \left[K\cdot(vgs + c\cdot vds(t) - vt)^2\right] & \text{otherwise} \end{cases}$$

EQ. (50)

where c = 0.5

$$id1(vgs, vds, t) := \begin{cases} K\cdot\left[2\cdot(vgs + c\cdot vds(t) - vt)\cdot vds(t) - vds(t)^2\right] & \text{if } vds(t) \le (vgs + c\cdot vds(t) - vt) \\ \left[K\cdot(vgs + c\cdot vds(t) - vt)^2\right] & \text{otherwise} \end{cases}$$

EQ. (51)

where c = 1.0

[0424] FIG. 49 illustrates the voltage relationship between Vgs and the aperture voltage for receiver 1902.

[0425] FIGs. 50-53 illustrate the frequency spectrums for the currents of FIG. 48. FIGs. 50-53 are logarithmic plots. FIG. 50 is a combined plot of the frequency spectrum for all three of the current plots of FIG. 48. FIG. 51 is a plot of the frequency spectrum for the current of a FET switching device of receiver 1902. FIG. 52 is a plot of the frequency spectrum for the current of a FET switching device of receiver a typical FET switching device. FIG. 53 is a plot of the frequency spectrum for the current of a FET switching device of receiver 2002. As can be seen in the plots, there is an absence of second order distortion for the FET switching device of receiver 1902.

[0426] As will be understood by a person skilled in the relevant arts, these plots herein demonstrate the enhanced linearity features of embodiments of the invention.

5 Example Method Embodiment of the Invention

[0427] FIG. 62 illustrates a flowchart of a method 6200 for down-converting an electromagnetic signal according to an embodiment of the present invention. This method can be implemented using any of the receiver and/or

transceiver embodiments of the present invention described herein. Method 6200 is described with reference to the embodiment illustrated in FIG. 16O. As described below, method 6200 comprises five steps.

[0428] In step 6202, a RF information signal is received. The RF signal can be received by any known means, for example, using an antenna or a cable. In embodiments, the RF signal may be amplified using a low-noise amplifier and/or filtered after it is received. These steps, however, are not required in accordance with method 6200.

[0429] In step 6204, the received RF information signal is electrically coupled to a capacitor. For the receiver shown in FIG. 16O, the RF signal is electrically coupled to the carrier(+) port of receiver 1602 and capacitor 1604. When used herein, the phrase "A is electrically coupled to B" does not foreclose the possibility that there may be other components physically between A and B. For receiver 1602, the received RF signal is inverted (e.g., using an inverter as shown in FIG. 17), and the inverted RF signal is coupled to the carrier(-) port and capacitor 1606. In embodiments (e.g., 2001), there is no need to invert the received RF information signal. Thus, the step of inverting the received RF signal is not required in accordance with method 6200.

[0430] In accordance with method 6200, the RF information signal may also be electrically coupled to a capacitor using a switching device coupled to the capacitor. For example, for receiver 1688 shown in FIG. 16H, the received RF signal is coupled to capacitor 1604 through switching device 1608. Similarly, the inverted RF signal is coupled to capacitor 1606 through switching device 1610. Thus, as will be understood by a person skilled in the relevant arts, two or more devices can be electrically coupled yet not physically coupled.

[0431] In step 6206, a switching device, electrically coupled to the capacitor, is used to control a charging and discharging cycle of the capacitor. In FIG. 16O, switching device 1608 is used to control the charging and discharging of capacitor 1604. As described above, when switching device 1608 is closed, the

RF signal coupled to capacitor 1604 causes a charge to be stored on capacitor 1604. This charging cycle is control by the apertures of control signal 1646, as described herein. During a period of time that switching device 1608 is open (i.e., between the apertures of control signal 1646), a percentage of the total charge stored on capacitor 1604 is discharged. As described herein, capacitor 1604 is sized in accordance with embodiments of the invention to discharge between about six percent to about fifty percent of the total charge stored therein during a period of time that switching device 1608 is open (although other ranges apply to other embodiments of the invention). In a similar manner, switching device 1614 is used to control the charging and discharging of capacitor 1606 so that between about six percent to about fifty percent of the total charge stored therein is discharged during a period of time that switching device 1610 is open.

[0432] In step 6208, a plurality of charging and discharging cycles of the capacitor is performed in accordance with the techniques and features of the invention described herein, thereby forming a down-converted information signal. The number of charging and discharging cycles needed to down-convert a received information signal is dependent on the particular apparatus used and the RF signal received, as well as other factors. Method 6200 ends at step 6210 when the received RF information signal has been down-converted using the techniques and features of the invention described herein.

[0433] In embodiments of the invention, the down-converted signal has a carrier signal riding on top of the down-converted signal. Thus, as described herein, this carrier signal can be removed, for example, by filtering the down-converted signal or by amplifying the down-converted signal with a band-limited amplifier. For the embodiment of the invention shown in FIG. 16O, the carrier signal riding on the down-converted signal is removed using amplifiers 1620 and 1624. As will be understood by a person skilled in the relevant arts, amplifiers 1620 and 1624 are intended to operate on signals having a lower range of frequencies than carrier signals. Thus, amplifiers 1620 and 1624 act as filters to a carrier signal riding on top of a down

converted signal. In embodiments of the invention, a low pass filter is used to remove the carrier signal as described herein, and as would be known to a person skilled in the relevant arts.

6 Conclusion

[0434] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.